CDF Run IIb Trigger & Data Acquisition Upgrades

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for the CDF Collaboration

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Run IIb Trigger/DAQ Upgrades

Outline:

- Motivation
  - Run IIb physics goals
  - Trigger strategies
  - Upgrade Strategy and process
- Specific projects
  - Status
  - New Scope
- Schedule
- Cost
- Conclusion

The upgrades:

1.3.1 TDC replacement
- Central tracker readout

1.3.2 Level 2 trigger
- Level 2 decision crate

1.3.3 (1.3.11) XFT upgrade
- Level 1 track trigger

1.3.4 Event builder

1.3.5 Level 3 Processor
- Data acquisition

1.3.6 SVT
- Level 2 silicon vertex trigger

1.3.7 Silicon DAQ

Trigger/DAQ Management

Motivation

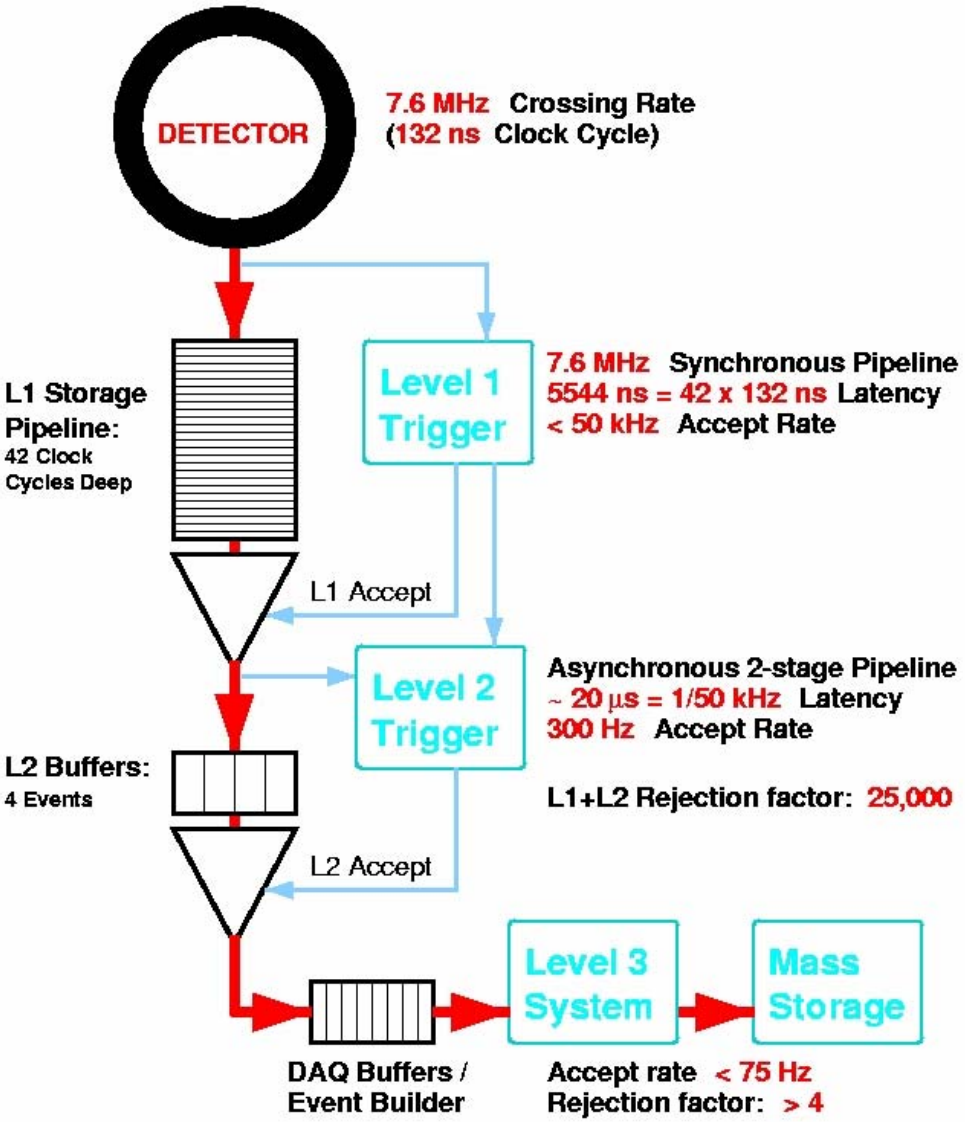
- The DAQ/Trigger upgrades presented here were originally driven by the Run IIb trigger and data acquisition needs to carry out our high-p_T physics program. However, the need to maintain parts of the B-physics program (eg B_s mixing) in Run IIb pushes us in the same directions.
- At the baselining our understanding was based upon
  - **Run IIa data: L $\leq$ 2x10^{31} cm^{-2} s^{-1}, <1 interaction per crossing**
  - **Run I data: L ~2x10^{31} cm^{-2} s^{-1}, ~3 interaction per crossing**
- We are extrapolating to Run IIb
  - **L = 3x10^{32} cm^{-2} s^{-1}, ~8 interaction per crossing**
  - **Due to significant uncertainties in extrapolation, and a desire to be prepared for success, we have evaluated the bandwidth needs for: L = 4x10^{32} cm^{-2} s^{-1} , ~10 interaction per crossing**
- Now can make better extrapolations based on:
  - **Run IIa data: L $\leq$ 1x10^{32} cm^{-2} s^{-1}, ~2.5 interaction per crossing**

Trigger Strategy

- Focus on Higgs & high p_T searches
  - Know that triggers needed for these modes will allow for many beyond Standard Model searches
- Maintain B program to highest possible luminosity.
  - ~1/2 data accumulated with $L_{inst} < ½ L_{peak}$
- General requirements:
  - High p_T electrons and muons
    - Associated *WH*/*ZH* modes, also $t \rightarrow Wb$
  - Missing E_T triggers
    - $\boldsymbol{ZH}$ **with** $\boldsymbol{Z \rightarrow \nu\nu}$, modes with taus
  - *b*-jet triggers
    - $\boldsymbol{H \rightarrow bb}$, *b*-jets tagged by displaced tracks
  - Calibration triggers
    - $\boldsymbol{Z \rightarrow bb}$, $\boldsymbol{J/\psi \rightarrow \mu^+\mu^-}$, photons
  - Hadronic B Triggers
    - $\boldsymbol{B \rightarrow h^+h^-}$, $\boldsymbol{B_s \rightarrow \phi\phi}$, $\boldsymbol{D_s\pi}$, two displaced tracks

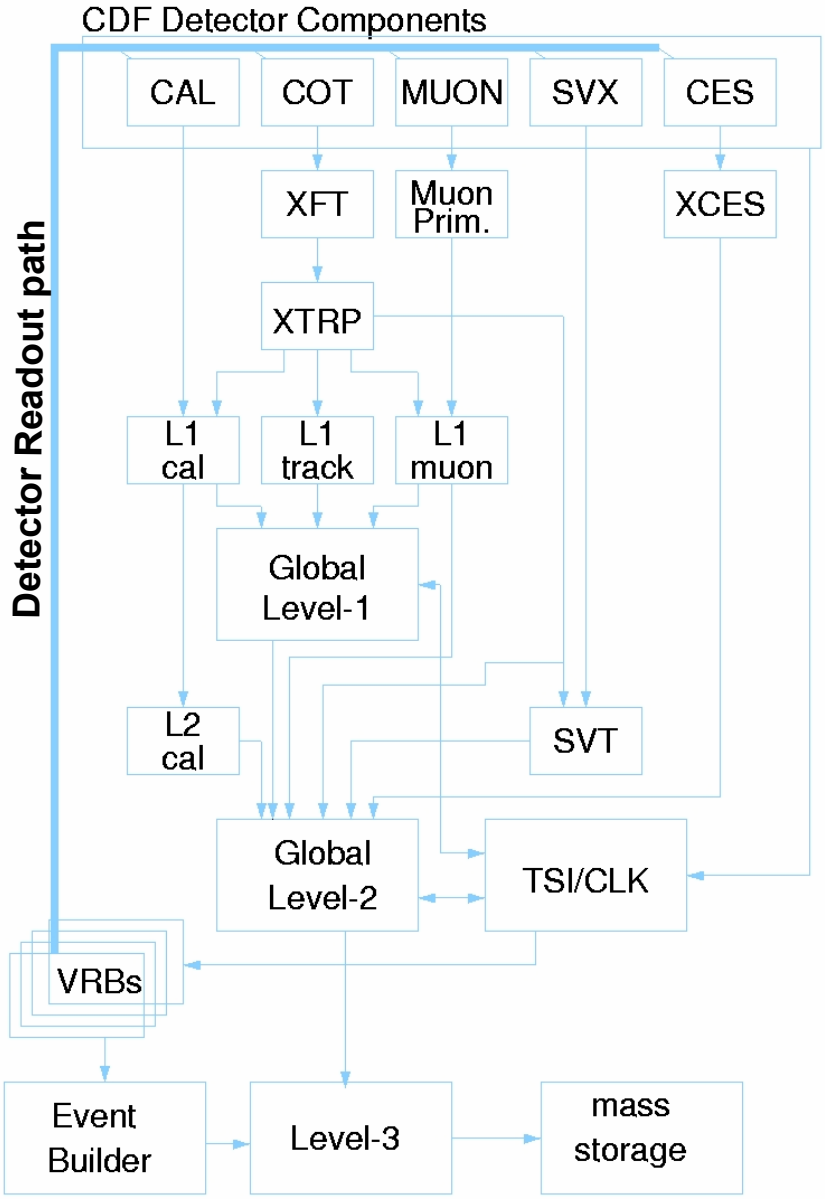
CDF Data Acquisition System

- Level 1 trigger
  - pipelined and “deadtimeless”
  - fully synchronous
  - designed for 132ns operation
  - on L1A, write data to 1 of 4 local L2 buffers
- Level 2 trigger
  - asynchronous
  - L1 + supplemental info
- Level 3 trigger
  - full detector readout
  - PC farm runs reconstruction
  - output to mass storage



CDF Run II Trigger System

- Level 1 trigger
  - tracking
  - calorimeter: jets & electrons
  - muons
- Level 2 trigger
  - L1 information (tracks, μ)
  - calorimeter clustering for jets and electrons
  - calorimeter shower max
  - silicon information
  - algorithms run in L2 processor
- Level 3 trigger
  - full detector readout
  - "offline" processing



Run IIb Trigger Table (High p_T part)

From Sep. 2002 DOE Review: extrapolated from L~2×10^{31} cm^{-2} s^{-1}

trigger path	σ_{L1}(nb)	σ_{L2} (nb)	σ_{L3} (nb)
High E_T electron	1,500	170	30
Plug electron + missing E_T	771	55	10
High P_T muon (CMUP)	1,773	200	8
High P_T muon (CMX)	1,773	200	8
2 high pT *b*-jets	10,840	200	10
missing E_T + 2jets	163	126	13
jets	6,500	42	12
missing E_T	overlap	163	3
Photons	overlap	50	15
$J/\psi\rightarrow\mu^+\mu^-$	850	38	10
High P_T jets	19,000	60	17
hadronic top	overlap	50	5
di-τ	5,000	50	4
missing E_T+τ	overlap	50	4
High E_T photons	13,500	110	21
dileptons, trileptons	1,000	190	45
total	**59,200**	**1904**	**215**
rate @4E32	**25kHz**	**750Hz**	**85Hz**
rejection factor	**~100**	**~33**	**~9**

DAQ/Trigger Specification Run IIa vs IIb

	Run IIa Specification	Run IIa Achieved	Run IIb Specification
Luminosity	8.6×10^{31}	9.0×10^{31}	30×10^{31}
L1 Accept	45 kHz	25 kHz	30 kHz
L2 Accept	300 Hz	350 Hz	1000 Hz
Event Builder	75 MB/s	75 MB/s	500 MB/s
L3 Accept	75 Hz	80 Hz	100 Hz
Rate to Storage	20 MB/s	20 MB/s	40 MB/s
Deadtime Trigger	5%	10%	5% + 5% †

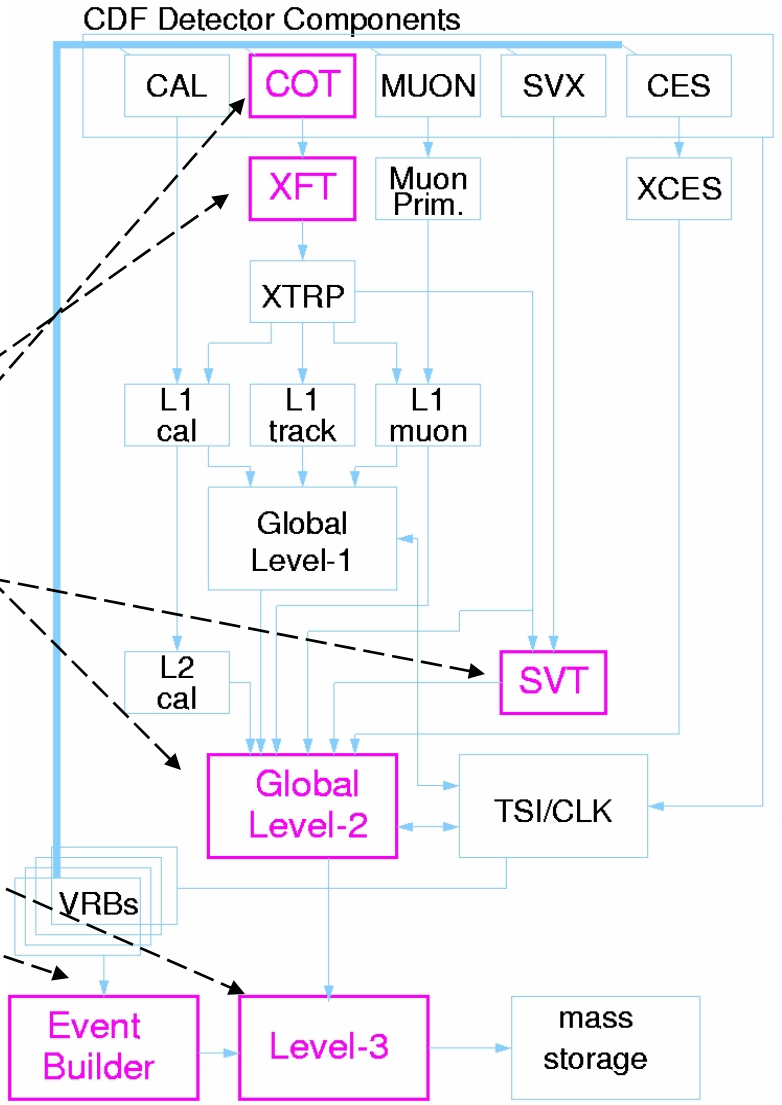
- Run IIa L1A not achieved due to higher than specified Silicon Readout + L2 Trigger execution times

† Assume ~5% from readout and ~5% from L2 processing

- Reminder: IIb trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)

Trigger/DAQ Upgrades for Run IIb

- Need to Maintain or increase bandwidth
  - ↑Luminosity ➔ ↑ Rate (=σ∗L)
  - ↑Luminosity ➔ ↑inter/x-ing
    ➔ ↑Complexity (and fakes)
    ➔ ↑Event Size, ↑Exec. time and ↑$\sigma_{trigger}$
  - All ↓$\sigma_{physics}$ to tape
- L1 Bandwidth (output to L2)
  - XFT ➔↑Purity ➔↓$\sigma_{trigger}$(L1, L2)
  - SVT, L2 ➔↓L2 Exec. t ➔↑L1 Bandwidth
- L2 Bandwidth (output to L3)
  - COT TDC ➔↑Readout rate
  - Level 3 Processing ➔↓L3 Exec. t
  - Event Builder ➔↑Readout rate
- L3 Bandwidth (output to tape)
  - CSL ➔↑Tape rate (not under IIb project)



General DAQ Upgrade Considerations

- Upgrades "targeted" to specific needs
  - *e.g.* COT TDCs replaced, but COT front-end (ASDQ, repeaters) unmodified
- Retain existing infrastructure
  - Cables, crates unchanged
  - I/O protocols, timings retained
- Upgrades plug compatible with existing components and where possible designed for parasitic commissioning
  - Use IIa knowledge & experience
  - Upstream/downstream components unchanged
  - Can install each system when ready with minimal interruption to operations
  - Minimize impact of commissioning on on-going data taking

DAQ/Trigger Upgrade Process

- Each subproject within the DAQ/Trigger has followed/will follow a similar path (not all steps apply in each case)
  - Conceptual design
  - Simulation/Tests of conceptual design
  - Internal Review of conceptual design
  - Technical specification
  - Construct/buy prototype/preproduction hardware and test
  - Readiness review for production purchase
  - Checkout and system test of production hardware
  - Installation readiness review
- Each subproject also holds weekly internal project meetings for technical and management discussions

Recent Reviews and Workshops

Over the past few months several projects have been through reviews and workshops in this process. Since upgrades will have an impact on operations, these workshops and reviews planned in coordination with CDF Operations Department.

- 1.3.1 TDC
  - (Pre)Production Readiness Review - May 21, 2004
- 1.3.2 L2 Decision
  - Production Readiness Review – Nov 7, 2003
- 1.3.3 (1.3.11) XFT
  - Scope Review – May 25, 2004
  - Scope and Project Plan Review – June 25, 2004
- 1.3.4 Event Builder
  - Production readiness review – April 2004
- 1.3.6 SVT
  - Workshops – April 28, June 14, 2004
  - Scope and Plan Review – June 29, 2004

COT TDC Upgrade

Central Outer Tracker (COT)

- central drift chamber

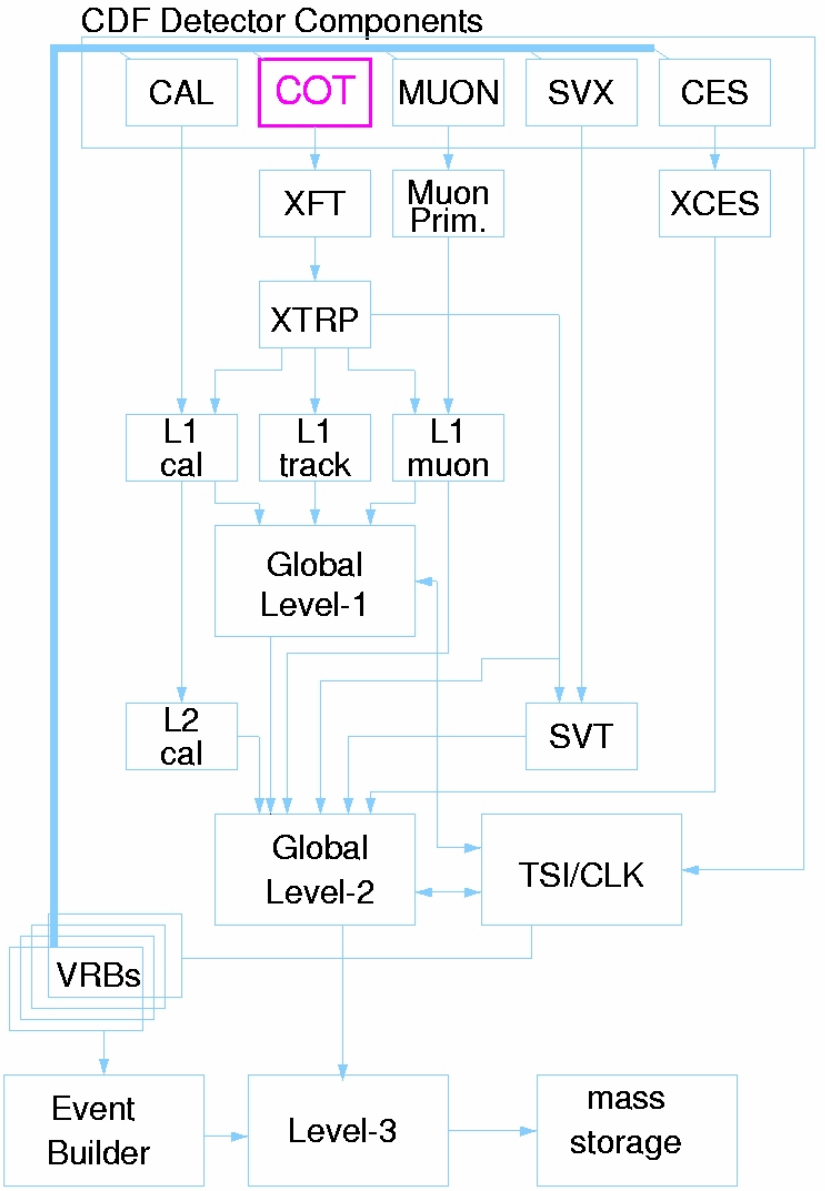
COT readout path:

chamber→ASDQ → microcoax → repeater board →flat cable →TDC

ASDQ = amplifier shaper discriminator with charge-encoding

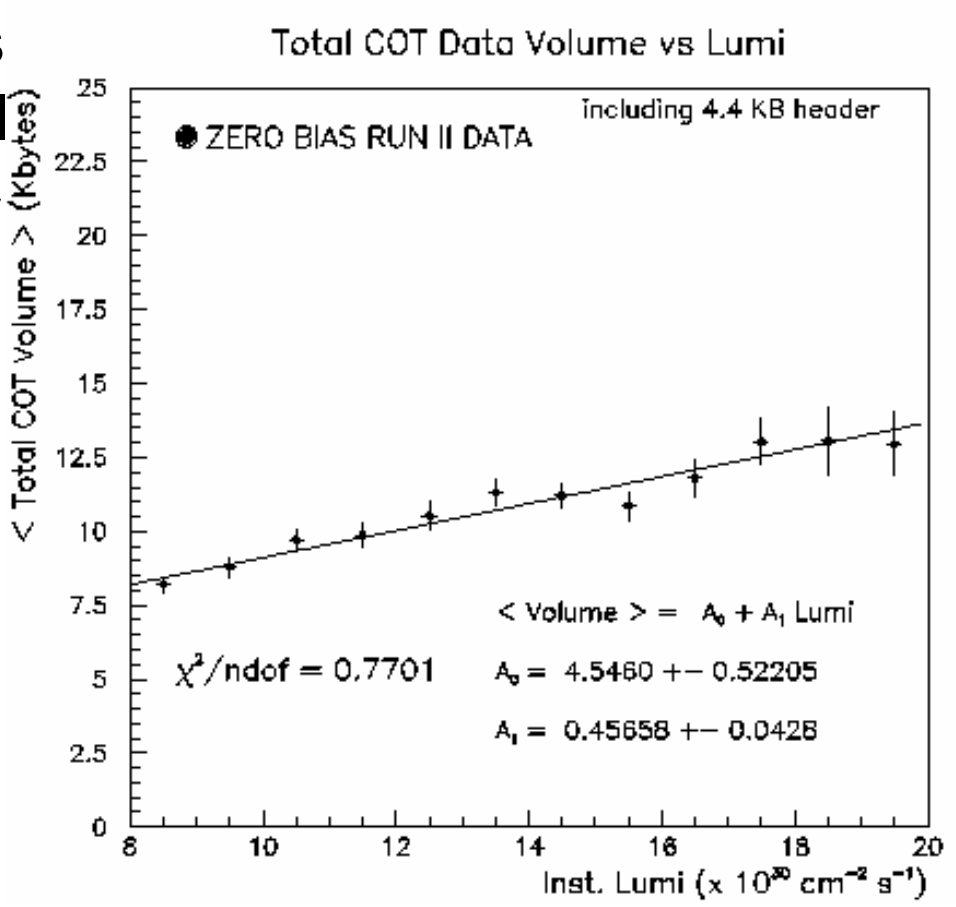
TDC = time-to-digital conversion

Total of 315 9U VME boards (96 channels each) to instrument full COT



COT Data Size

- Occupancy is higher than was expected before start of Run II
- Extrapolation (linear) from low luminosity (<$2x10^{31}cm^{-2}s^{-1}$) to $4x10^{32}cm^{-2}s^{-1}$ predicted:
  - 62.5 k hits/event for whole chamber or average of about 2 hits/wire/event
  - Average of about 4 hits/wire in SL1
  - Data size of 250 kB/event with 4 bytes/hit (current usage)
  - Average data rate of 14MB/s in each crate (assuming 1.1kHz L2A rate)

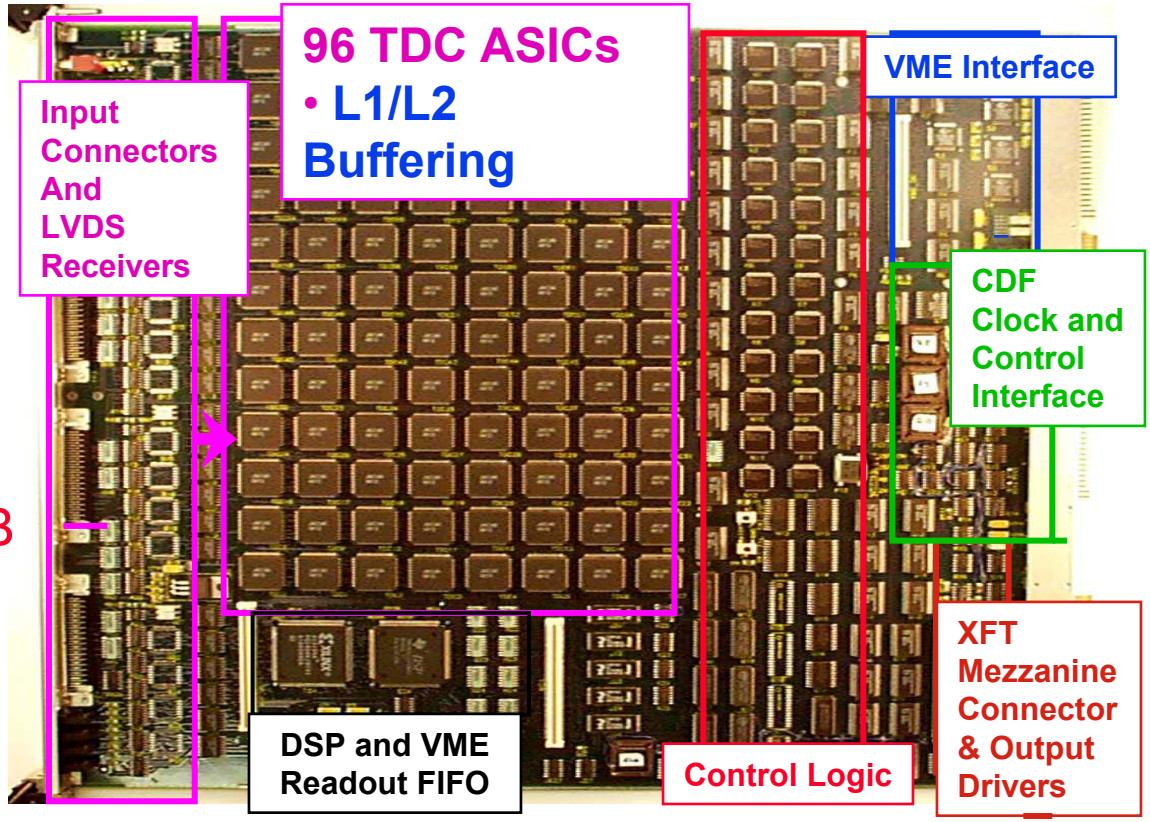


Occupancy confirmed by recent higher luminosity operation

Run IIa TDC Limitations

At time of Sep. 2002 DOE Review

- On-board processing (DSP) Time grows with # of hits
  - t = 1200μs/event for SL1 (4 hits/ch) at $4x10^{32}$ $cm^{-2}s^{-1}$
  - Pipelined w/readout
- VME Readout
  - 16 TDCs per crate
  - Read sequentially by one block transfer (~14MB/s)
- VME to Event Builder
  - TRACER →TAXI→VRB link limited to 12MB/s
- 2002 Internal review recommended pursuing replacement



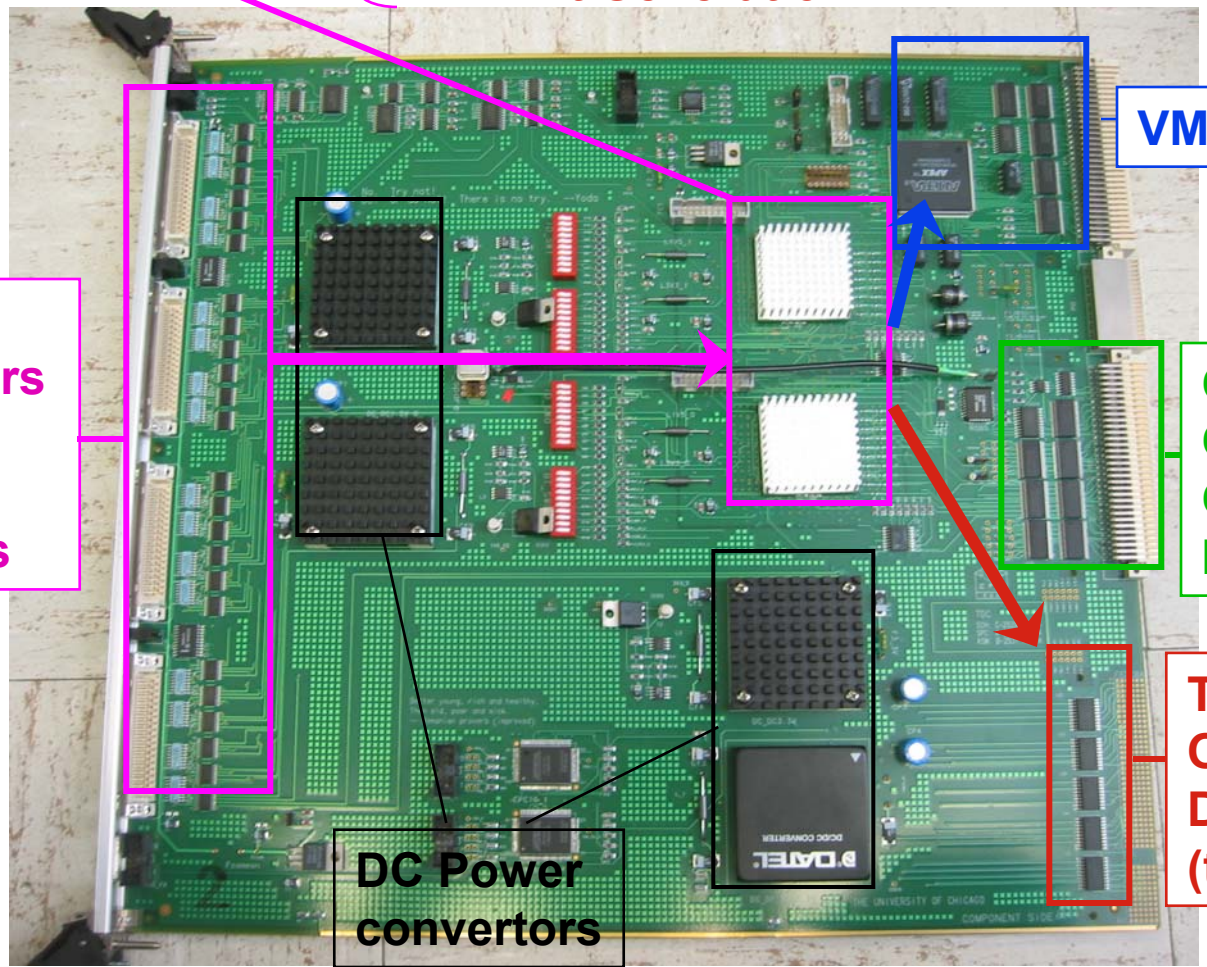
Run IIb TDC Specifications

- Backward compatible with existing system
  - No change to COT front-end, cables or calibration
  - No change to track trigger (XFT) interface
  - Accept CDF specific signals from CDF_CLOCK/TRACER
- Must handle the following rates
  - 50kHz L1A, 1.1kHz L2A
- Perform hit finding for track trigger
- "TDC Specifications" document on web site provides details

Run IIb TDC Design

Altera Stratix FPGAs
(48chan/chip)

840MHz Diff LVDS inputs
TDC: Serial to 10bit parallel conversion (1.2ns/bit)
L1/L2 Buffering, hit processing + Readout (CBLT)
XFT Hit Generation



VME Interface

Input Connectors And LVDS Repeaters

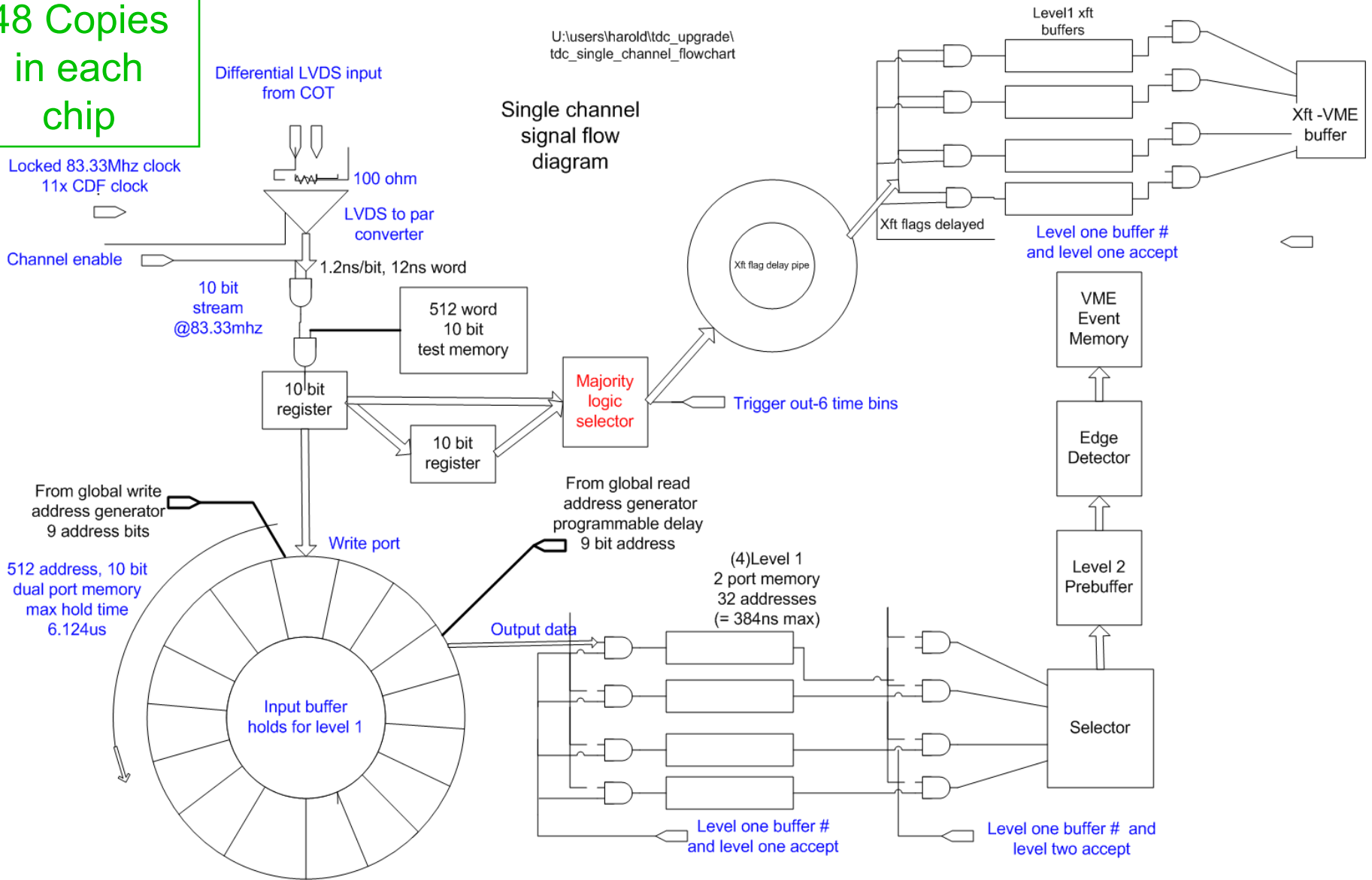
CDF Clock and Control Interface

Trigger Output Drivers (to XFT)

DC Power convertors

Block Diagram of a TDC Channel

48 Copies in each chip

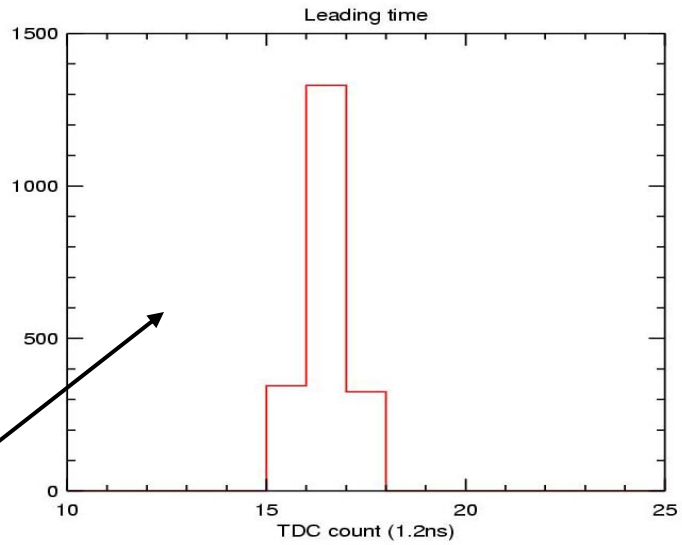


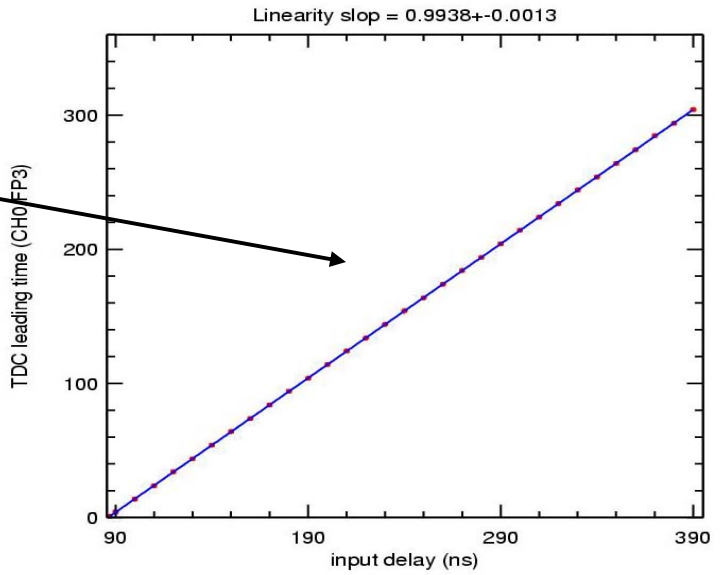
New TDC System Design

- Addresses on-board processing deadtime
  - Process 96 channels in parallel
  - <10μsec/event independent of occupancy (up to 7 hit/channel)
- Addresses VME Readout bandwidth
  - One Chained Block Transfer (CBLT) per crate → lower overhead
  - Compressed data size: 4 bytes/hit → 56 bytes + 2 bytes/hit. (14kB/crate/event → 8 kB/crate/event for $4 \times 10^{32} cm^{-2} s^{-1}$)
- Addresses TRACER → Event Builder (EVB) bandwidth
  - Gigabit Ethernet from crate CPU (Motorola 5500) to LINUX PC (Virtual VRB). Virtual VRB interfaces via gigabit Ethernet to upgraded EVB.
  - Independent of new TDC board, can install/commission separately
- Design exclusive to COT system, reduces constraints
  - Run IIa TDC will continue to work well for low occupancy systems (muons, hadron timing, CLC)

Status of Run IIb TDC

- Additional Manpower this year
  - FNAL EE and Comp Prof on testing
  - Duke physicists on installation/commissioning
- Four Prototype boards
  - Delivered Feb 2004
  - Only needed 1 “blue” wire modification to make them work
- Timing Performance meets or exceeds specification
  - Leading edge stability for 24 channels (dominated by ASDQ input variation)
  - Slope = (0.9938+/-0.0013 cnts)/1.2ns
  - Final measurements in progress
- A few issues with firmware for XFT outputs
  - Can be resolved within firmware
- Measured readout rate with CBLT – achieved 17MB/s



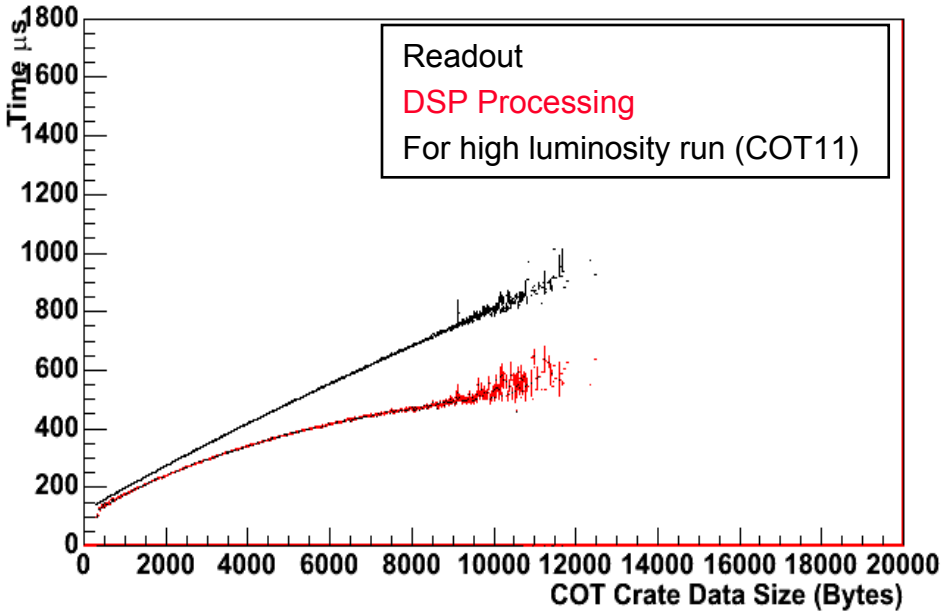


May 2004 TDC Readiness Review

- Charge:
  - Evaluate Run IIb TDC performance, plans for testing, Production, Installation
  - Also evaluate status and ultimate performance of Run IIa TDC
- Recommendations for IIb TDC design
  - Proceed with PreProduction ASAP – in progress
  - Complete tests of prototype boards in parallel – in progress
  - More testing with XFT, DAQ, full crate and COT – modified plans

Progress on Run IIa TDC

- New version of DSP code in use for several months is much faster:
  - Was 1270μs for 4 hits/channel
  - Now 740μs for 4 hits/channel
- Demonstrated that VME readout is slower than DSP
  - Event size is limitation



- Review committee recommendations for Run IIa TDCs
  - Adopt more compact IIb data format (~50% smaller) – In progress
  - Recommend understanding the ultimate performance of the Michigan TDCs in a timely manner - in progress
- Plan:
  - 07/04 Run IIa TDC Performance Workshop (next week)
  - 09/04 Run IIa TDC Performance Review

Run IIb TDC Progress

- ✓ July 2003 Design Review
- ✓ Feb 2004 First Prototype Board Ready for Testing
- ✓ May 2004 (Pre)Production Readiness Review
- ✓ June 2004 Order PreProduction Boards
- Oct 2004 Full crate test and tests with DAQ
- Nov 2004 Test Full crate w/COT&DAQ (shutdown)
- Dec 2004 Production Readiness Review
  First TDC Tester Card Assembled
- Mar 2005 TDC Production Checkout Begins
- June 2005 Installation Readiness Review
- July 2005 TDC Production Checkout completed

Project Milestones

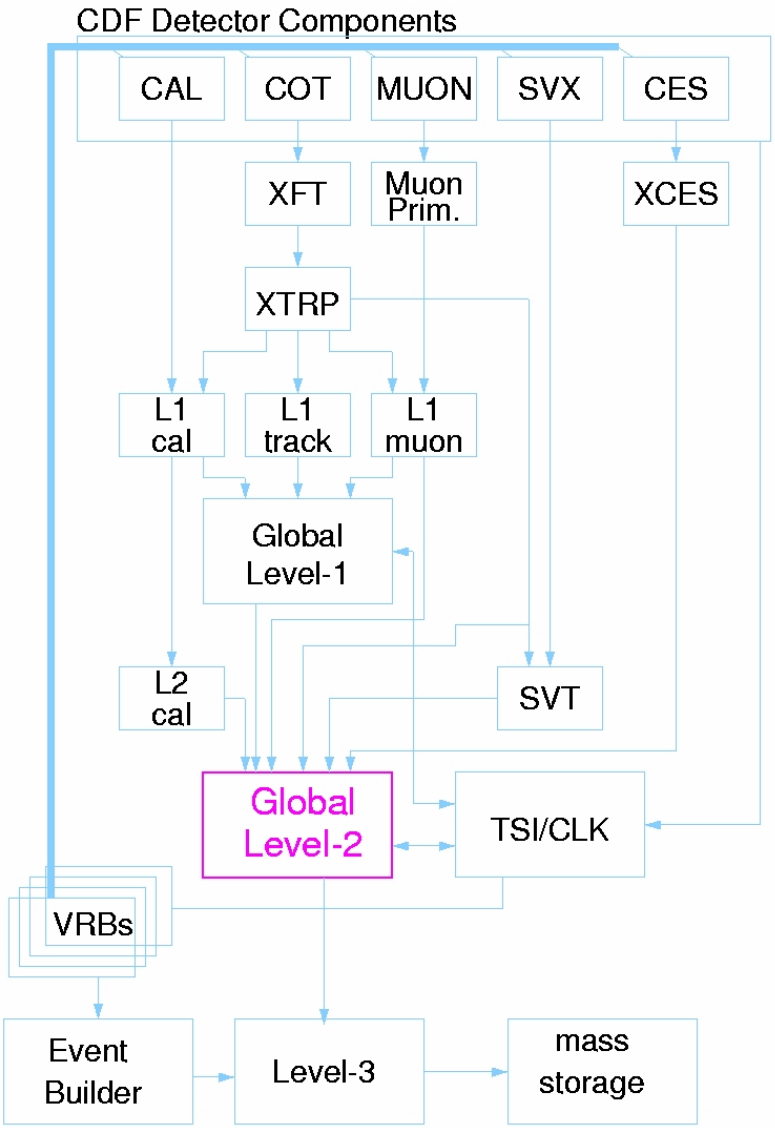
L2 Decision Crate Upgrade

Level 2 trigger decision based on information from:

- L1 trigger components
  - tracks, muons, missing E_T
- Jet clusters, EM clusters
- central strip chambers
- silicon

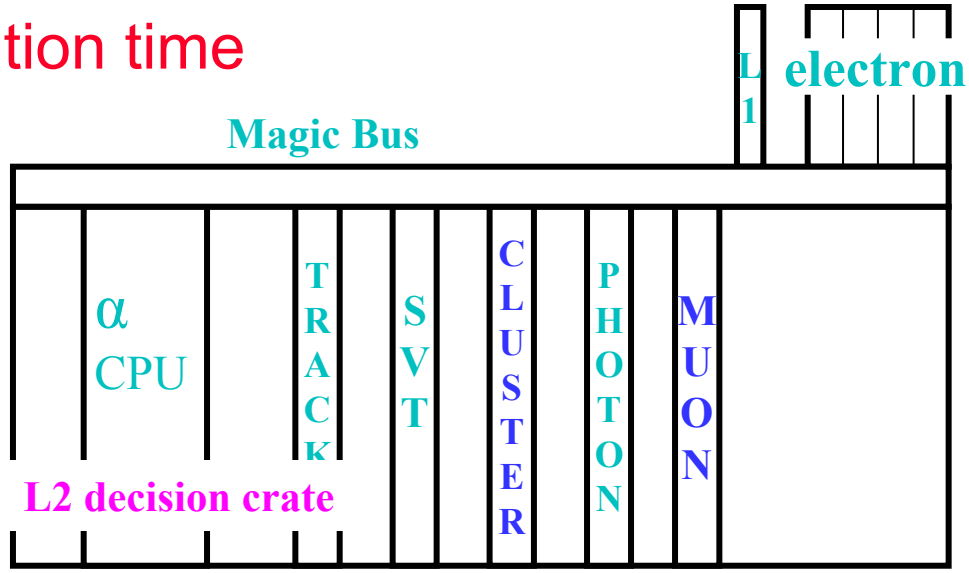
Information brought together and fed to processor(s) in the L2 decision crate

- L2 decision based upon trigger primitives
- high rate (up to 50kHz) in, must be fast



Run IIa Level 2 Decision Crate

- 6 flavors of interface board
  - (XTRP,SVT), L1, ISO, MUON, CES, Cluster
  - each uses different input format, different board designs
- 1 board with Alpha processor for L2 processing/decision
  - system designed to run with 4 Alphas
  - Data input with custom bus (MagicBus)
- Diversity makes system challenging to test & maintain
- DEC α processors obsolete
- Did not achieve design execution time
- CDF internal review recommended replacing Alphas for Run IIb
- Upgrade with PULSAR board as universal interface



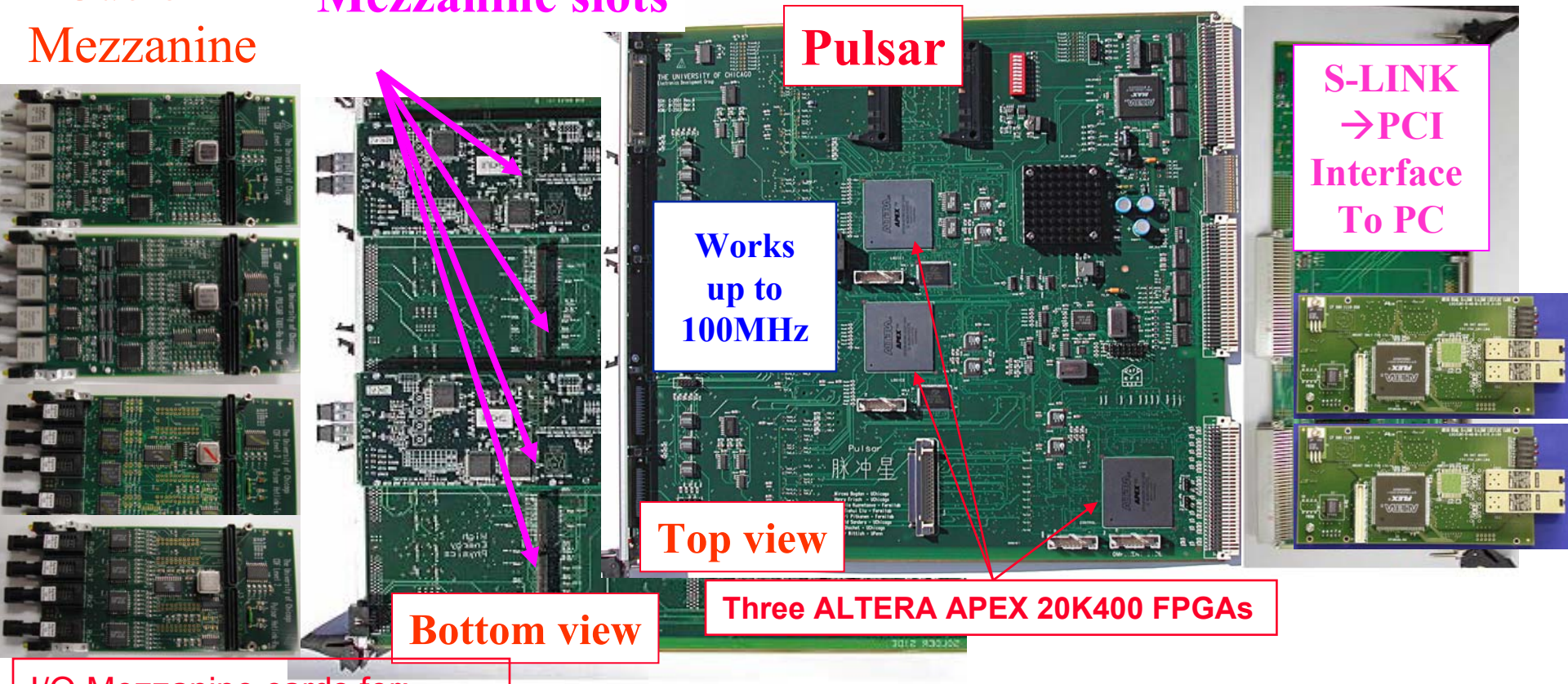
Pulsar (Pulser And Recorder) Design

Custom Mezzanine

Mezzanine slots

Pulsar

AUX card



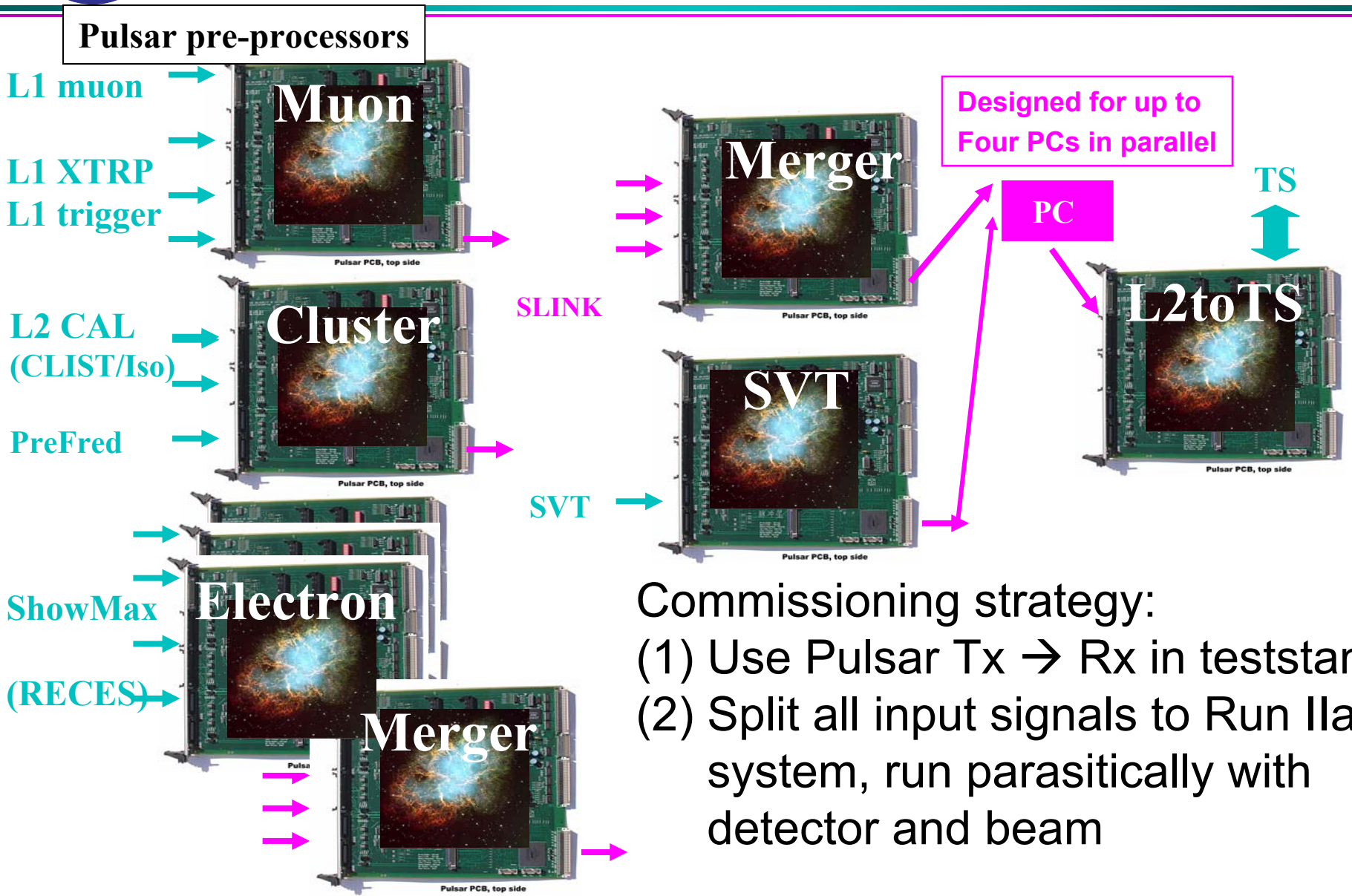
I/O Mezzanine cards for:

- S-LINK (CERN/LHC)
- Hotlink
- TAXI
- to be specified

Design philosophy:

- *Modular - interface with any link format*
- *Self-testable*

Pulsar based L2 decision



Commissioning strategy:

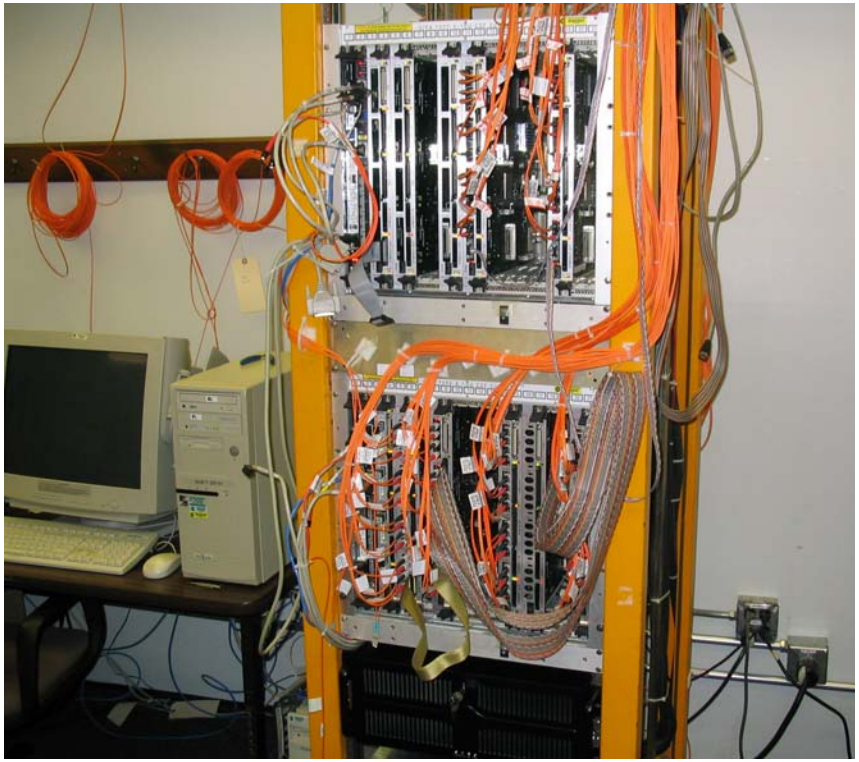
(1) Use Pulsar Tx → Rx in teststand

(2) Split all input signals to Run IIa system, run parasitically with detector and beam

Pulsars in Action

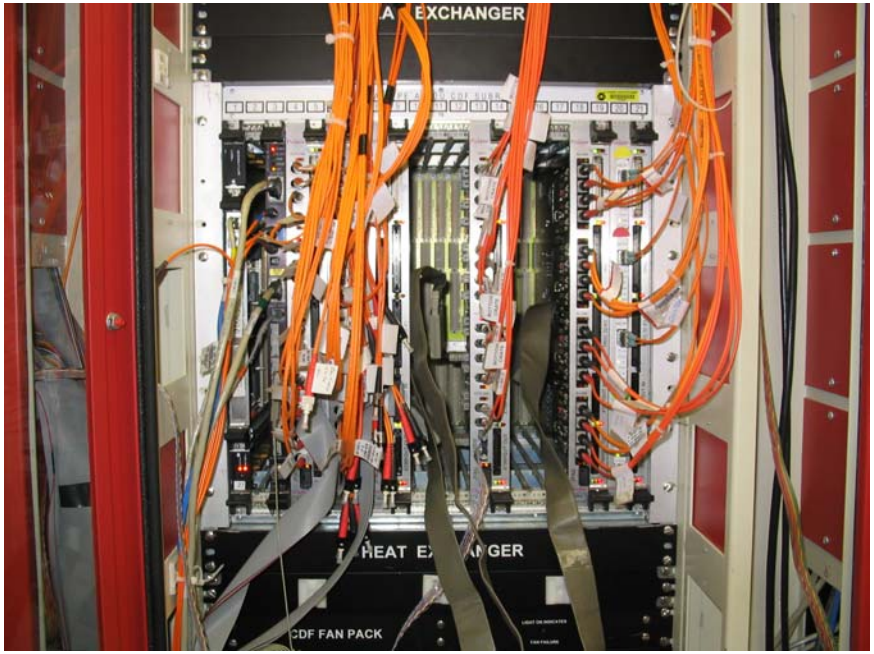
Two crate teststand in B0

With transmitter boards and receiver/interface boards



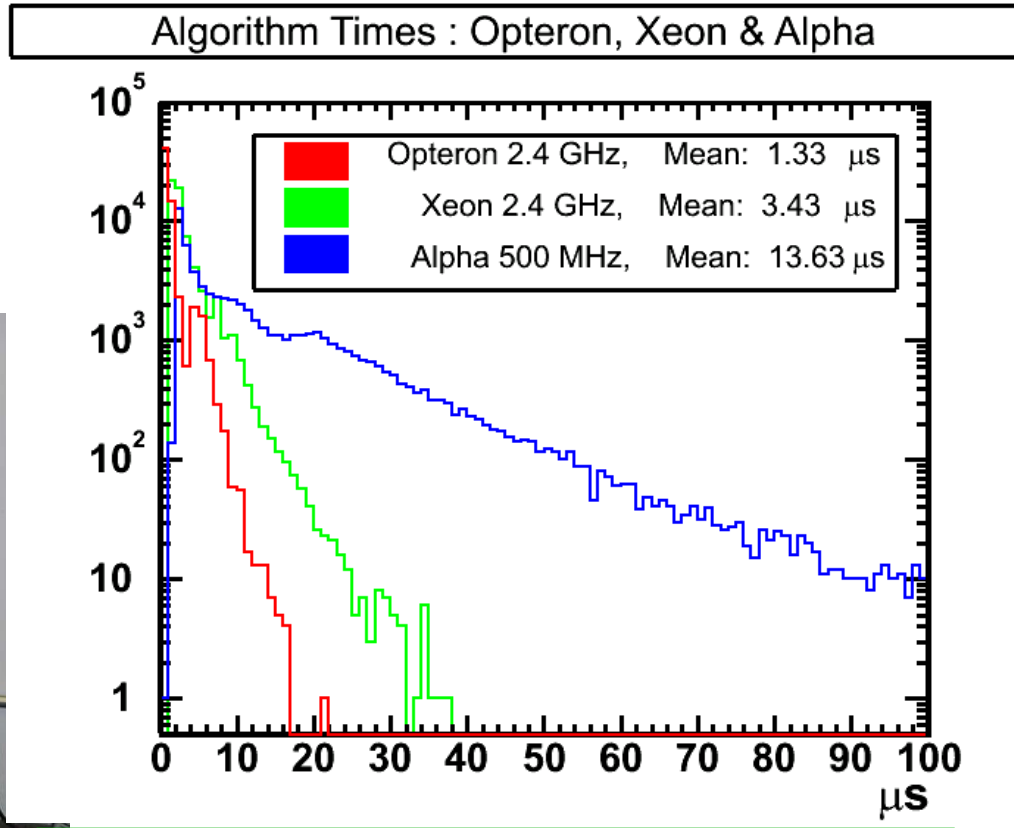
Run IIb L2 Decision (Pulsar) crate

In CDF Trigger Room



L2 Decision Processing time Measurements

PC with 2.4GHz AMD Opteron (64bit) Processor fed by SLINK from Pulsar system



Level 2 Trigger algorithms run on real data in Run IIa system compared to Run IIb PC

Complete time including loading over S-Link/PCI and returning result <10μs

L2 Decision Progress

- ✓ Sept 2003 Pulsar PreProduction Readiness Review
- ✓ Dec 2003 Pulsar PreProduction Complete
- ✓ Nov 2003 Pulsar Production Readiness Review
- ✓ May 2004 Pulsar Production Complete
- ✓ June 2004 Core Firmware Complete
- ✓ July 2004 Core Software Complete
- Sept 2004 Ready for Installation
- Fall 2004 Installation Readiness Review

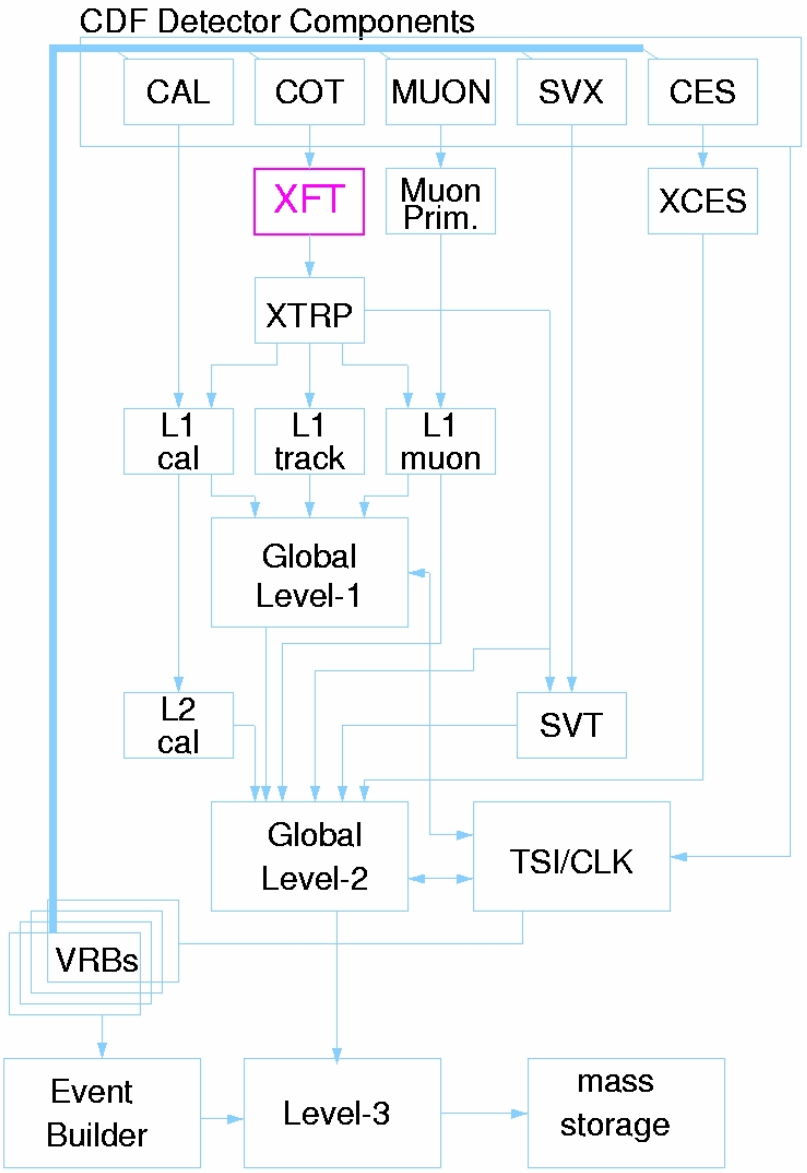
Project Milestones

eXtremely Fast Tracker Upgrade

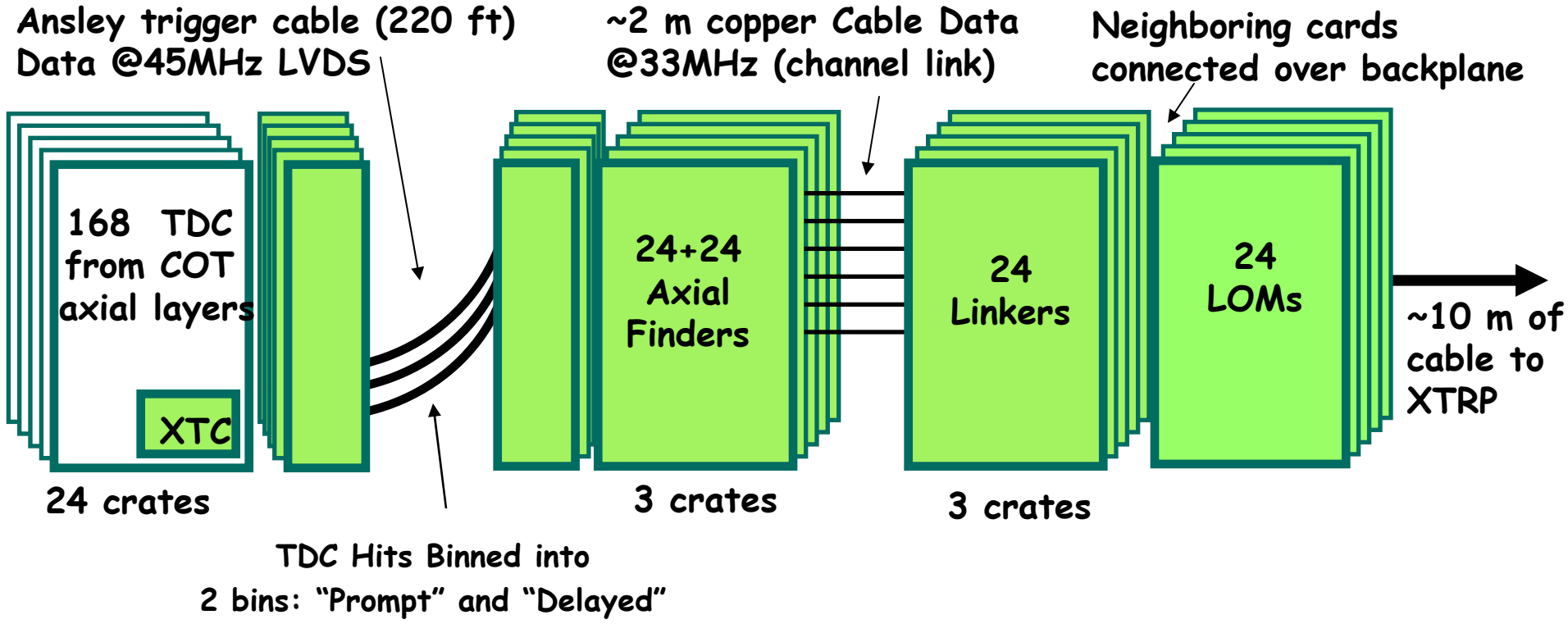
XFT finds charged tracks with $p_T > 1.5$ GeV/c

Part of the Level 1 Trigger system

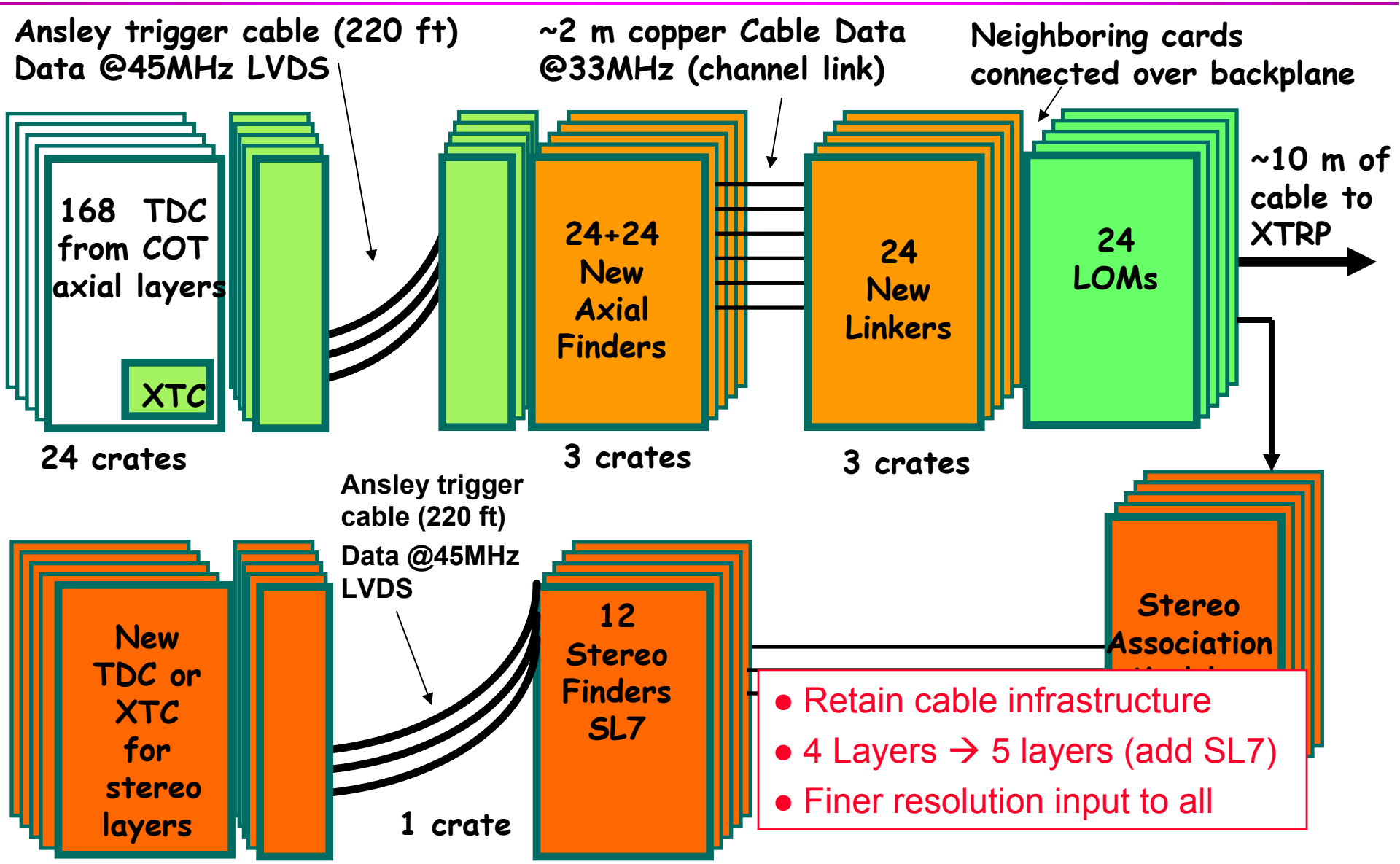
(more detail in afternoon breakout session)



Run IIa XFT Configuration



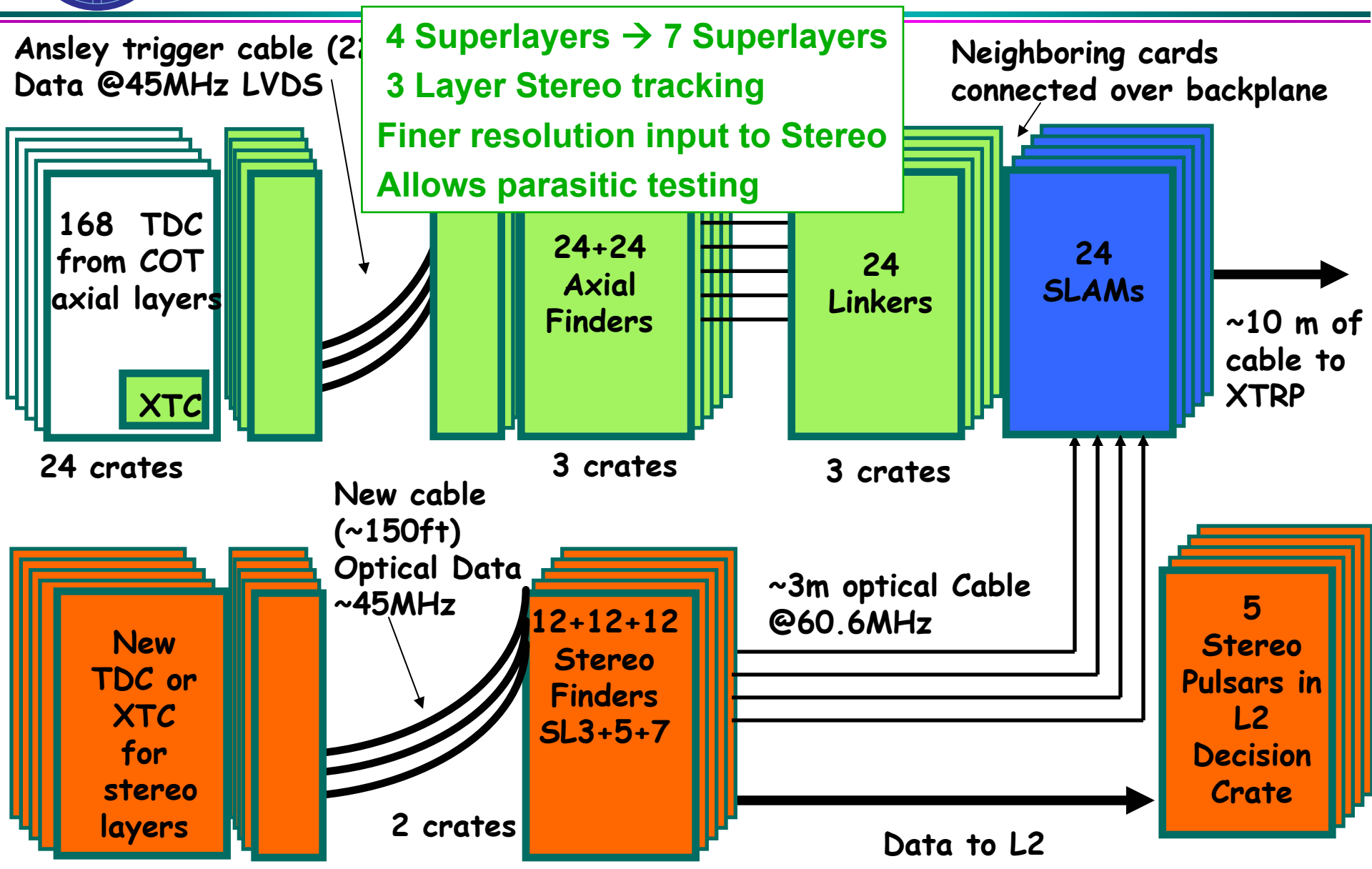
Baseline XFT Upgrade



XFT II Scope Reviews

- Two reviews (5/21 and 6/21) to evaluate performance and scope of the XFT upgrade and recommend course of action.
  - Progress was slow, problems discovered
  - Not enough good Ansley cables (TDC to XFT) to instrument stereo SL7
- Significant progress in last 9 months
  - Four new postdocs and three engineers join project
- More realistic simulations (and experience with Run IIa XFT)
  - Merge raw COT data from zero bias events to model high luminosity.
  - Reproduces trigger rates of recent higher luminosity operation
  - Performance degradation of IIa system smaller than original projections
- Committee Conclusions
  - Simulations demonstrate that baseline upgrade can achieve goals
  - Baseline upgrade no longer feasible, given the time available to complete project.
  - Consensus (Committee, XFT proponents, Run IIb management) that addition of more stereo (SL 3, 5 and 7) is the most reasonable course.

Re-scoped XFT Upgrade

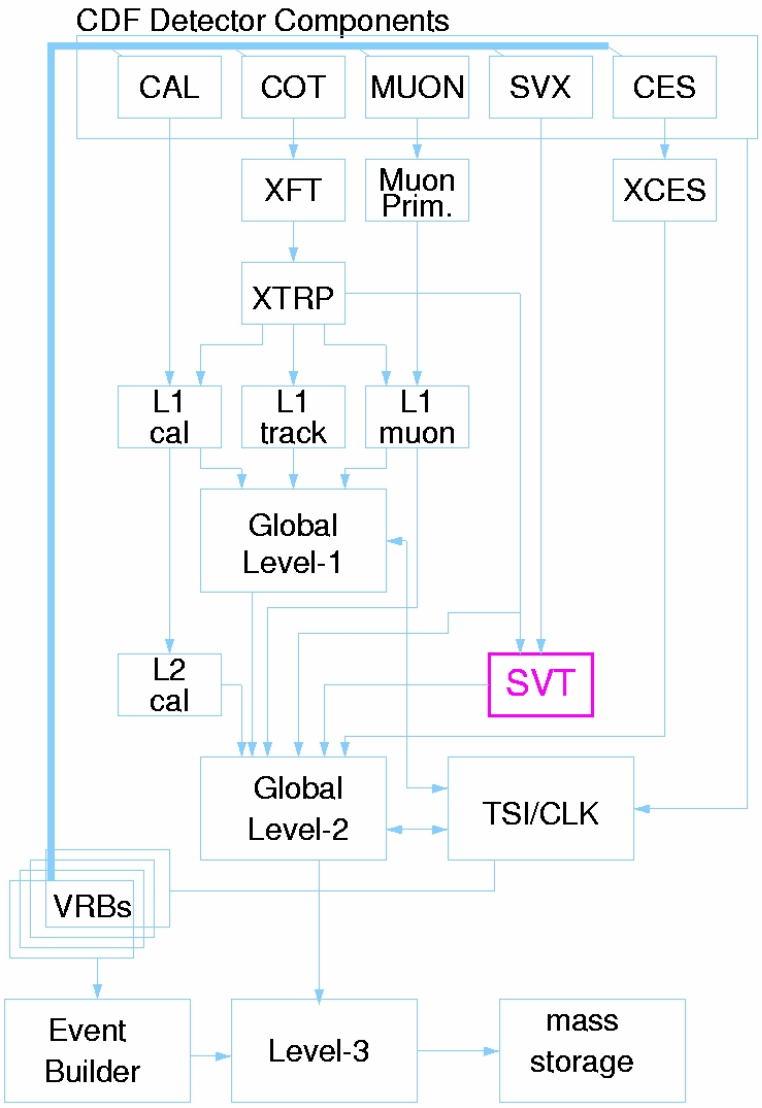


SVT Upgrade

Silicon Vertex Tracker (SVT)

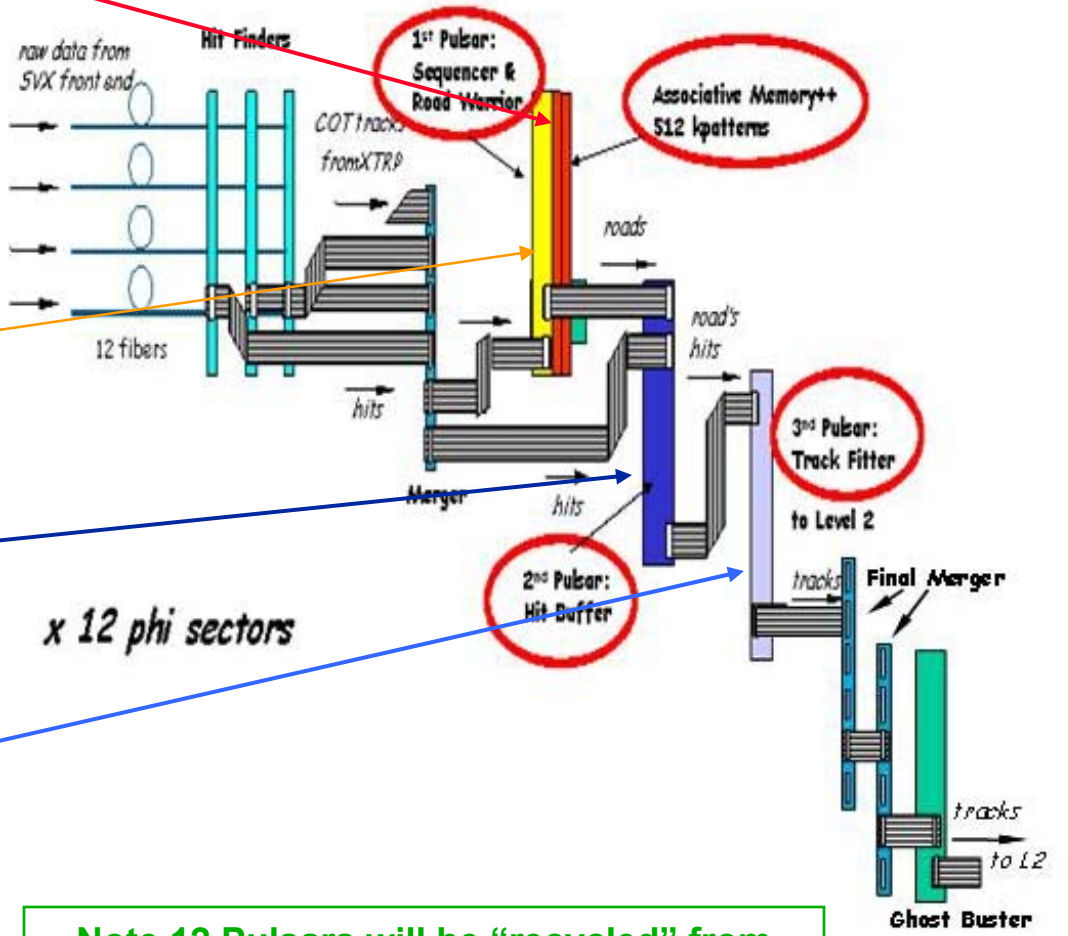
- brings axial silicon information into trigger
- allows for cuts on impact parameter at Level 2 in trigger (!)

- In order to be fast, SVT must specifically handle
  - SVX readout and geometry
  - Tevatron beam position
- Original Run 2B upgrade scope
  - Geometry change for Run 2B Silicon
- Upgraded boards would also speed up L2 Decision
- New scope review 6/29/04



Re-scoped SVT Upgrade

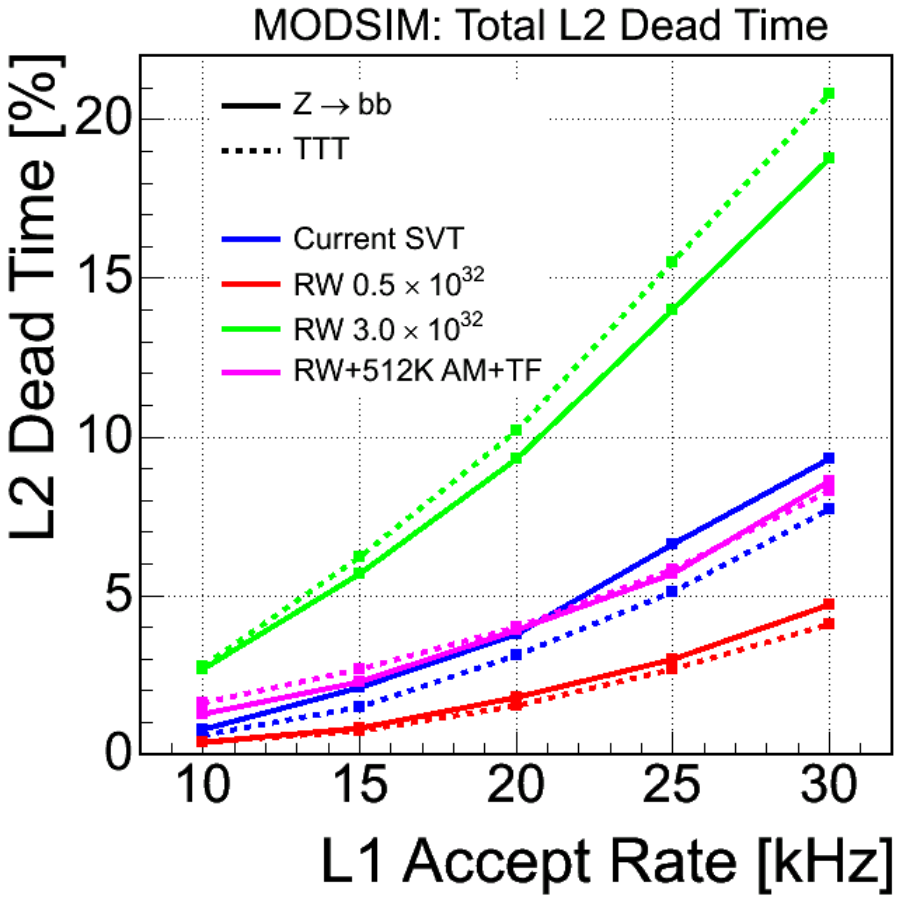
- New AM++ hardware with narrower roads (32K to 512K) reduces number of tracks to fit
  - Bought by INFN
- New AMSequencer/Road Warrior (12 Pulsars)
  - Interface for AM++
- New Hit Buffer (12 Pulsars)
- Faster Track Fitters reduce processing time on found roads (12 Pulsars)



Note 12 Pulsars will be "recycled" from current use as "Road Warrior" boards

Expected SVT Performance

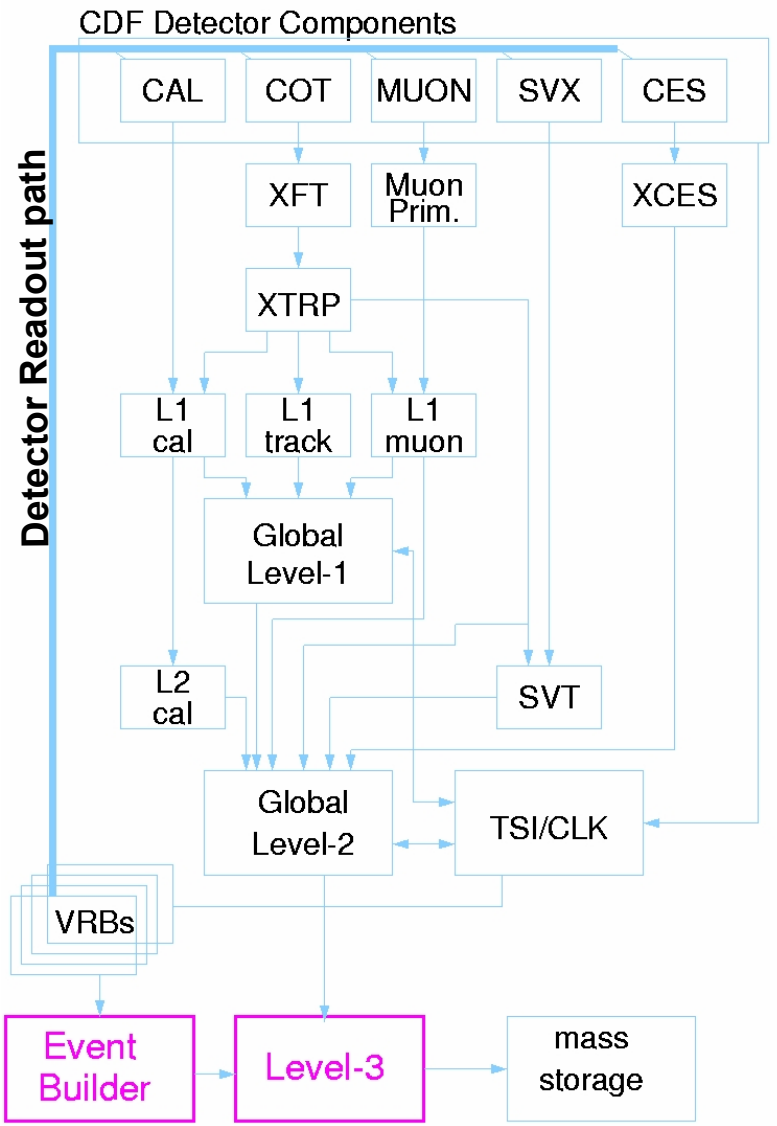
- SVT execution time has a large impact on L2 Trigger latency
  - Last data to get to L2 (can't start until after Si r-ϕ Readout)
  - Higher Si occupancy at high luminosity will increase processing time just when we need to decrease it
- Simulation (MODSIM) of CDF DAQ/Trigger:
  - L2 Upgraded SVT at 3×10^{32} has same bandwidth capability as pre-upgrade at 0.5×10^{32}
- More detail in afternoon Breakout Session



Event Builder/L3 Upgrade

Full detector readout occurs on Level 2 trigger accept

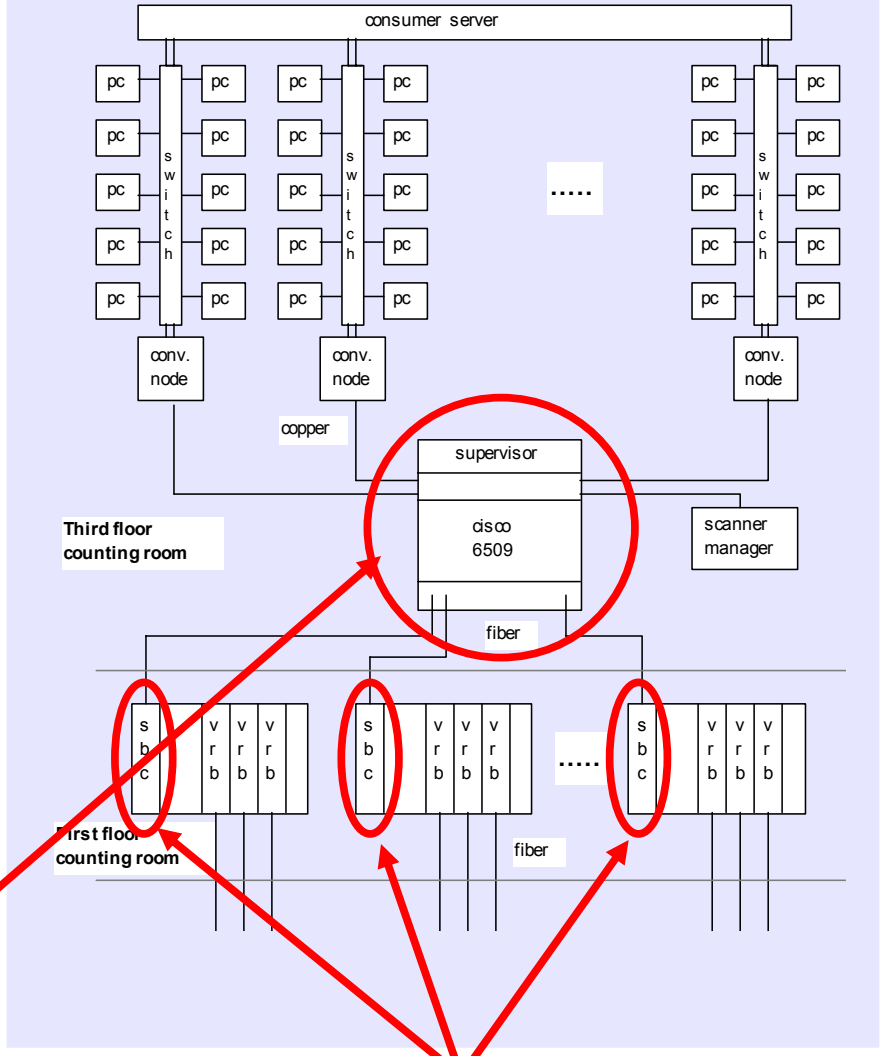
- Event Builder
  - subsystems send data to VRBs in VME crates
  - Event builder accepts data from VRBs, assembles the full event
- Level 3 Trigger
  - event sent: EVB→L3 PC farm
  - single PC node per event runs reconstruction & trigger algorithms
  - greater rejection at L3 needed in Run IIb



Run IIb Event Builder Upgrade

	RunIIa	Run IIb
Rate:	300Hz	1kHz
Event size:	250kB	500kB
Throughput:	75MB/s	500MB/s

SCPU:	MVME2600	VMIC7805
SCPU OS	VxWorks	Linux
Switch:	ATM	Cisco 6509 (gigabit ethernet)



new Cisco 6509 switch

new software (much less than IIa)

new VMIC 7805 boards (SCPUs)

Event Builder Teststand

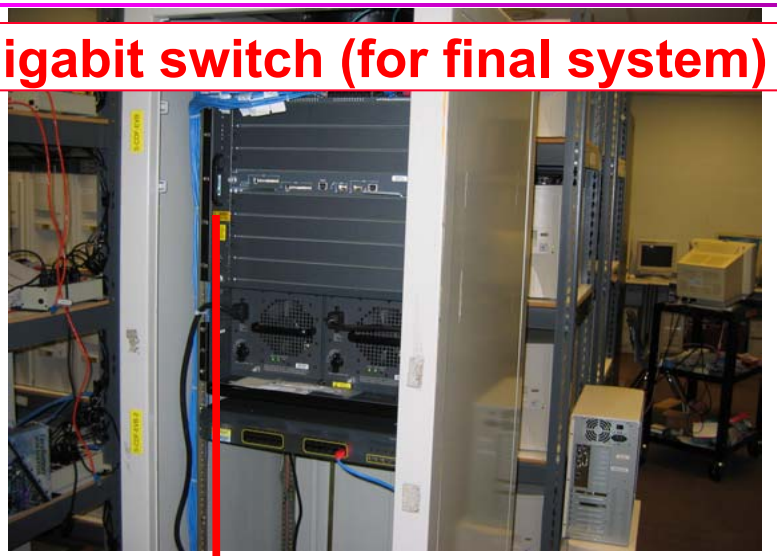
Test stand exists in B0

Code development ongoing

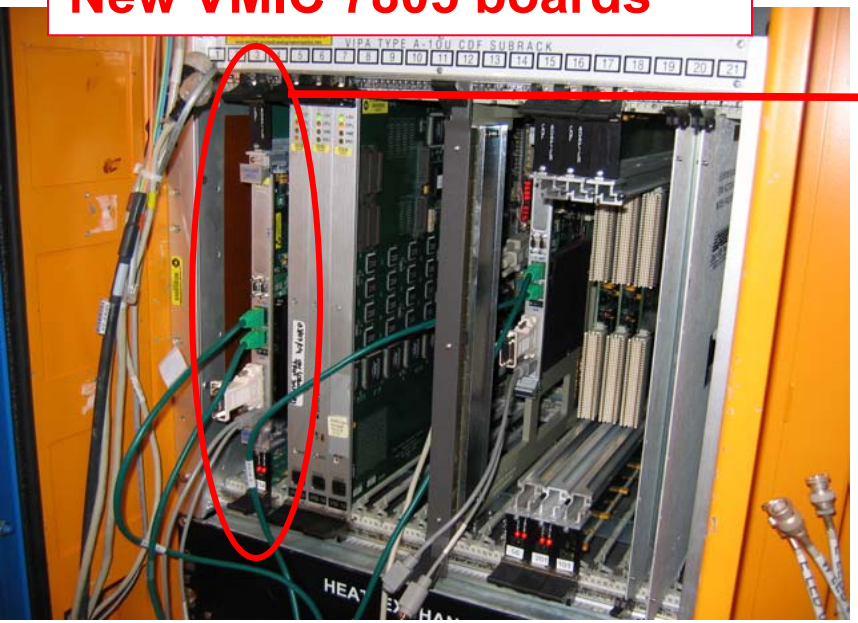
VRB → Switch →L3 Processor

- **36MB/s achieved**
- **30MB/s specification**

Gigabit switch (for final system)



New VMIC 7805 boards



VRB crate

"L3" nodes

Event Builder Progress

- ✓ Sept 2003 Switch technology choice, place order for final system switch
- ✓ Jan 2004 Arrival of final system switch, install test stand
- ✓ Apr 2004 Production Readiness review
- ✓ May 2004 SCPU choice, place order for final system SCPUs, complete code design
- Sept 2004 Arrival of final system SCPUs, code skeleton complete, start of testing during shutdown
- Jan 2005 Completion of Shutdown testing
- May 2005 Code complete, system ready for installation
- May 2005 Installation Readiness Review
- Sept 2005 Run IIb Event Builder installed

Project Milestones

CDF Trigger/DAQ Labor

- TDC
  - Chicago (ENG+TECH), Fermilab(ENG+PHYS+TECH), Duke(PHYS)
- XFT
  - Ohio State(ENG+PHYS+TECH), Illinois (ENG+PHYS+TECH), Purdue (PHYS), Fermilab (ENG+TECH), Baylor (PHYS)
- Level 2
  - Fermilab(ENG+PHYS+TECH), Chicago(ENG+PHYS+TECH), Penn(ENG+PHYS+TECH)
- SVT
  - Pisa(ENG+PHYS+TECH), Chicago(ENG+PHYS+TECH), Fermilab(PHYS), Ferrara(PHYS), Sienna(PHYS), Tsukuba(PHYS), LBNL(PHYS), Rome(PHYS), Wisconsin(PHYS)
- EVB/L3
  - MIT(PHYS), Fermilab(ENG)

Engineering/Technician Labor

- Key to completion of the SVT, TDC, and XFT projects in <14 months will be maintaining engineering effort
  - Efforts of Chicago, Fermilab, Illinois, INFN and Ohio State
- TDC
  - 2 EEs from Chicago on firmware and TDC Test card design
  - EE and CP from PPD/EED on TDC testing and software, firmware for TDC Test card
  - Technicians from CD/ESS (PREP) for checkout and maintenance
- SVT
  - Engineer from Chicago to design mezannine card
  - Engineer from Fermilab for Pulsar Firmware
- XFT
  - EE and technician from OSU for SLAM board design, layout
  - 2 EEs from Illinois for XTC mezannine card and TDC transition card
  - 2 EEs, layout technician and CP from PPD/EED for Finder design, layout and testing

DAQ/Trigger Project Schedule

	TDC	L2	XFT	EVB	SVT
WBS	1.3.1	1.3.2	1.3.11(3)	1.3.4	1.3.6
Conceptual Design					
Review					
Technical Design			10/04		10/04
Prototype & Test			N/A		N/A
Review			N/A		N/A
PreProduction & Test	12/04		3/05	N/A	
Review	12/04		3/05	N/A	
Production & Checkout	1/05-7/05		1/05-8/05		10/04-3/05
Installation Review	6/05	1/05	7/05	5/05	7/05
Install & Commission	8/05-10/05	3/05	8/05-10/05	5/05-8/05	8/05-10/05

Complete	
In Progress	Completion Date
Not Yet Started	Start - Finish Dates

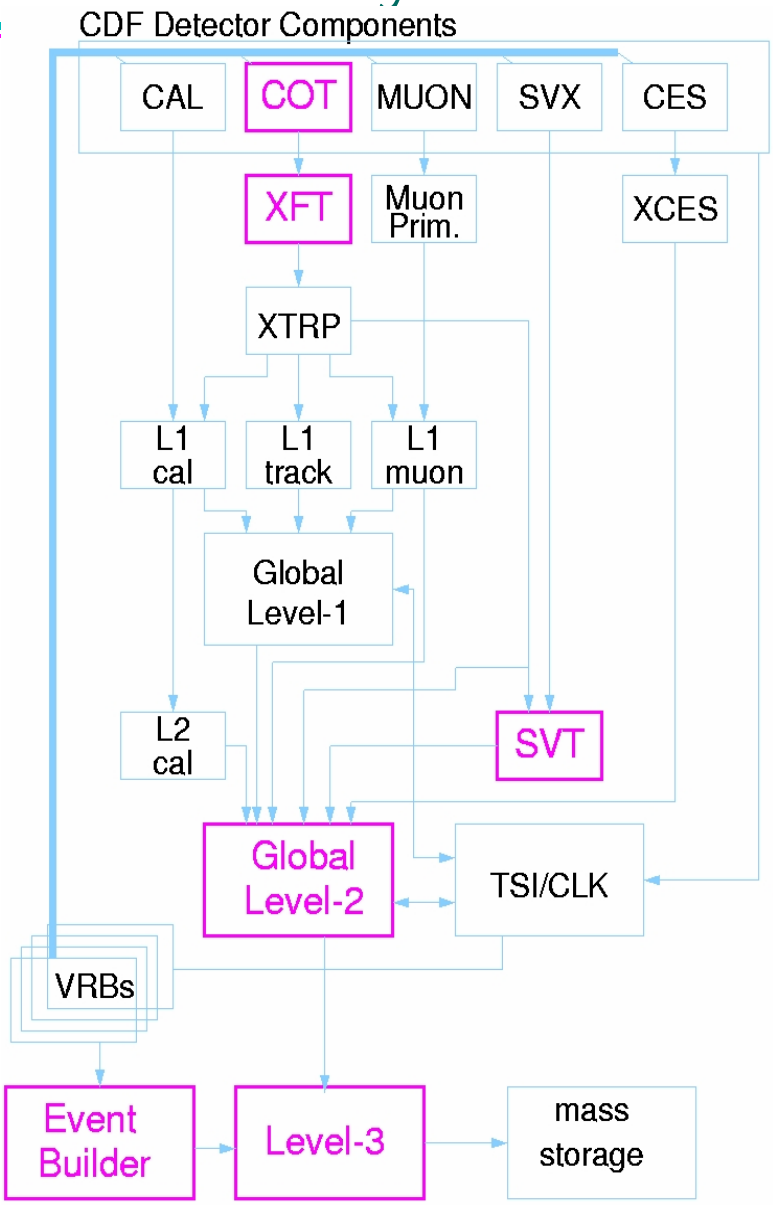
Cost by Subproject

Total Costs listed in AY dollars:

Run 2b DAQ and Trigger Project	Current Baseline (AY$)	Proposed Revised Baseline (AY$)	Change (AY$)
1.3.1 Run 2b TDC Project	1,105,744	1,135,589	29,845
1.3.2 Run 2b Level 2 Project	366,655	363,797	(2,858)
1.3.11(1.3.3) Run 2b XFTII Project	1,146,971	1,443,213	296,242
1.3.4 Event-Builder Upgrade	517,361	512,966	(4,395)
1.3.5 Computer for Level3 PC Farm / DAQ	478,908	478,908	0
1.3.6 SVT upgrade	174,441	296,430	121,989
1.3.7 Silcon Detector DAQ Upgrades	854,289	0	(854,289)
Totals:	4,644,369	4,230,903	(413,466)

DAQ/Trigger Summary

- With these upgrades to the CDF Front-end, Trigger and Data Acquisition system we obtain the bandwidth needed to carry out the Run IIb physics program.
- In production or production complete:
  - L2 Decision replacement
  - Event builder/L3 upgrade
- Nearing production:
  - COT TDC replacement
- New scope/big increase in effort
  - XFT upgrade
  - SVT upgrade
- The remainder of the Run IIa CDF front-end/trigger/DAQ system will perform well throughout Run IIb



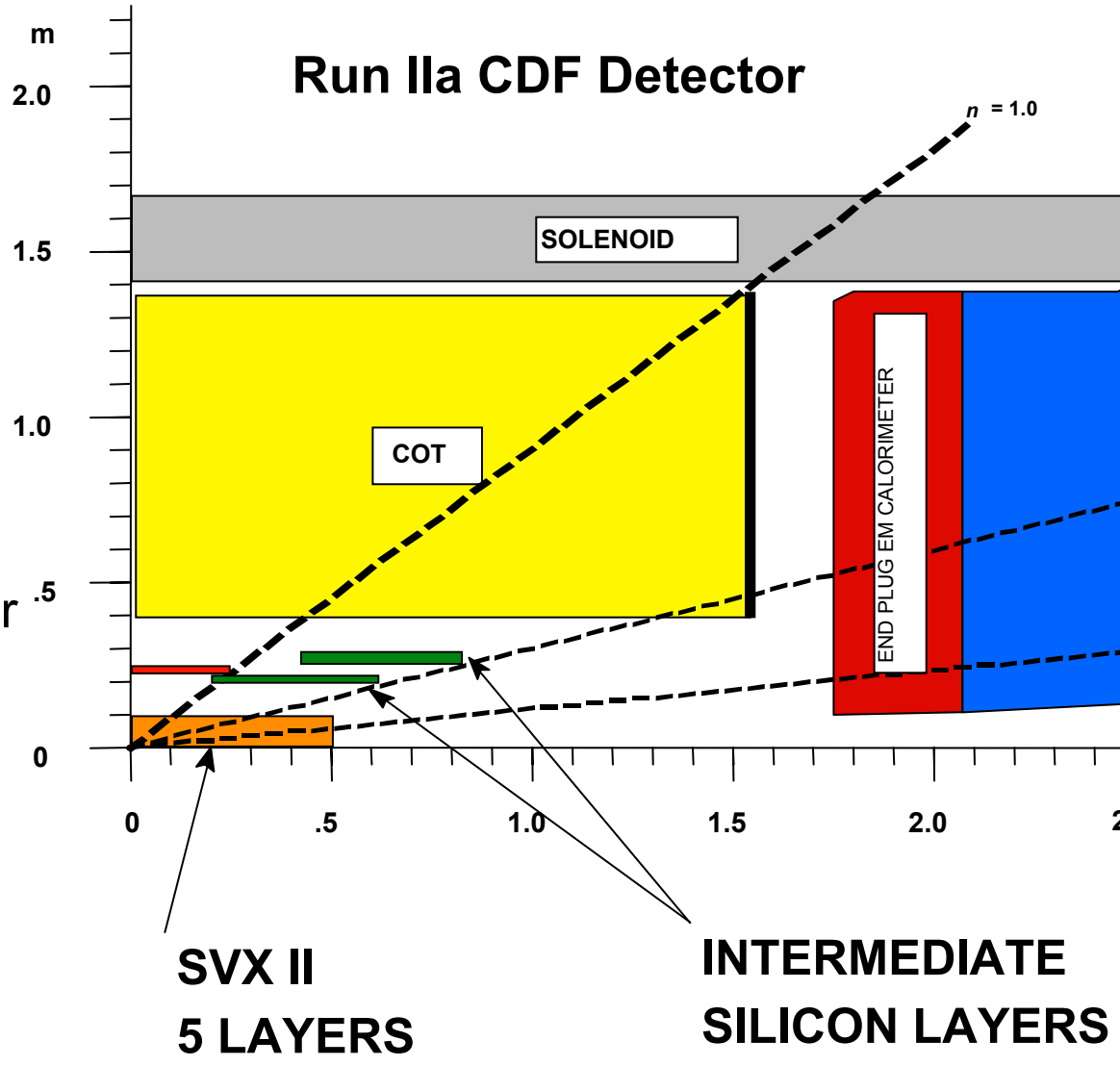
Additional supporting Slides

Supporting Documentation

- CDF Run IIb Technical Design Report
- Report from DAQ review Oct 2003
- TDCs
  - Specification for Run 2b TDC
  - CDF6998 – Run IIB TDC-II Address Space
  - CDF6999 – TDC-II Design and Specification – Run IIB TDC for the COT
  - May 2004 Production Review Report
- L2 Trigger
  - PULSAR Web page (documentation, schematics, BOM): http://hep.uchicago.edu/~thliu/projects/Pulsar
  - CDF6259: “Run IIb Upgrade for CDF L2 Decision Crate”
  - Nov 2004 Production Readiness Review Report
- XFT
  - CDF7039 XFT Upgrade Options and Studies
  - CDF6059 Specifications for the Upgraded XFT System for High Luminosity Running in Run 2
  - May 2004 Review Report
  - June 2004 Review Report
- SVT
  - CDF7064 Silicon Vertex Trigger Upgrade
  - Review report from June 2004 review
- EVB
  - Report on Prototype test results – April 2004
  - Report on review by DAQ Experts – April 2004

The CDF Detector

- Important detector element for this talk is the Central Outer Tracker (COT)
  - drift chamber with 30k sense wires
  - solenoid field is 1.4T
  - track needs p_T~75 MeV to get to COT inner layer
  - tracks with $|\eta|<1$ pass through all COT layers
  - inner layers see tracks with $|\eta|<2$



Limitations of Run IIa TDC

At time of Sep. 2002 DOE Review

- TDC on-board hit data processing
  - 96 channels processed serially by Digital Signal Processor (DSP) after L2A
  - Time (=deadtime) grows with # of hits → at $4x10^{32}cm^{-2}s^{-1}$ in SL1 processing takes 1200μsec/event (4 hits/channel)
  - Run IIa processing time too large for Run IIb specification
- VME readout
  - Hit processing for next event can occur during VME transfer for previous event
  - 16 TDCs per crate read out serially by VME block transfer
    - current VME transfer rate 14MB/s with additional overhead per board
    - Run IIa, 300Hz…falls to ~150Hz (!) in Run IIb
- Data transfer
  - TRACER→TAXI→VRB link is a bandwidth limitation
    - maximum TAXI →VRB is <12MB/s…Run IIb requires 14MB/s
- Internal CDF TDC Review committee (June 2002) ***Conclusion:***
  - Existing COT TDCs + VME readout system cannot maintain L2A rate in Run IIb
  - TDC system must be replaced **OR** significant modifications to the DAQ & infrastructure must take place

XFT IIb Design

From Sep. 2002 DOE Review

- **Reduce fakes and improve resolution with improved axial track finding & 3D information**
- Take advantage of existing design and infrastructure
  - Cables, I/O, data formats unchanged
- Difference between XFT & offline tracking is time binning. Segment angle match improves with finer time bins.

Upgrade:

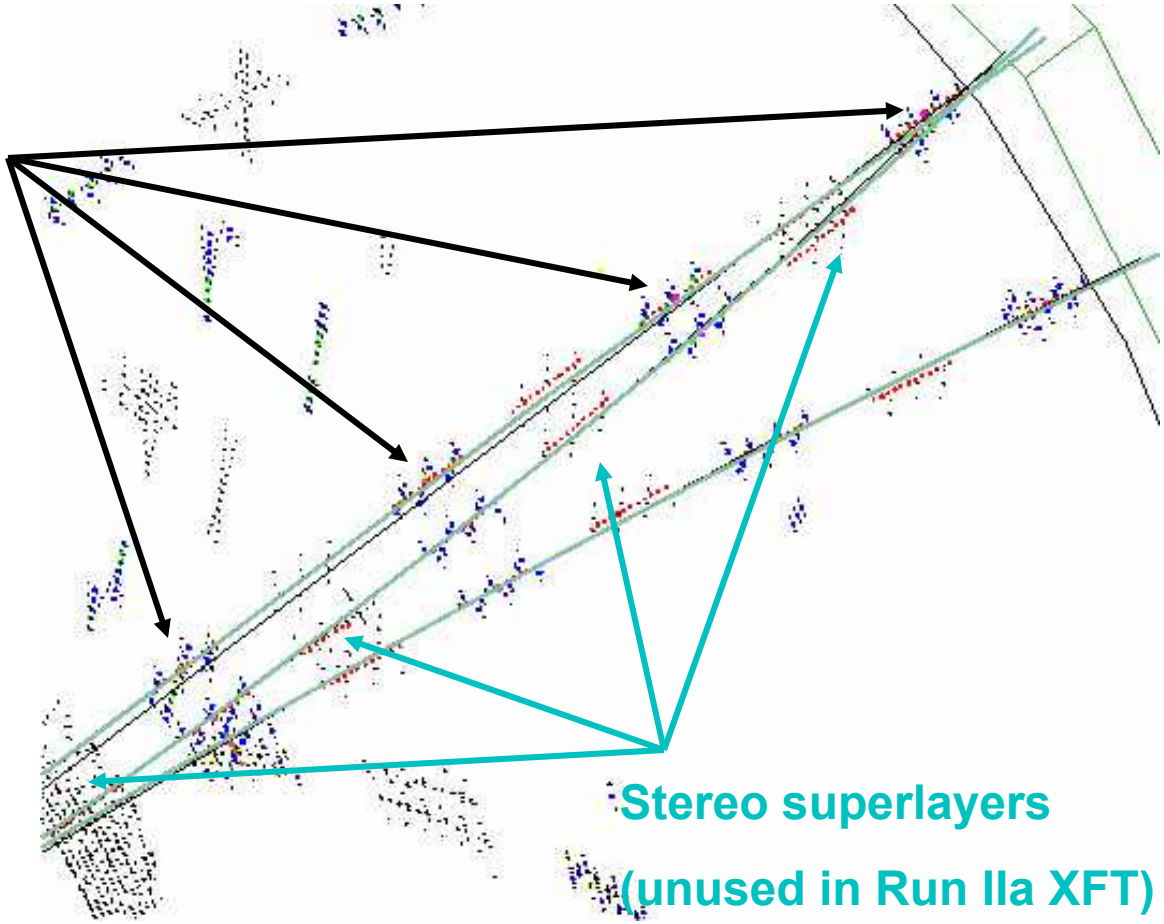
- Utilize 396ns baseline to pipe more information per beam-X from TDC→XFT.
  - Go from two time bins to six time bins in the trigger
- Supplement axial tracking with stereo measurement
  - Segment finding identical to axial XFT
  - Stereo information provides:
    - improved fake track rejection (important at high L)
    - new: electron & muon matching in η

Status of L2 Decision Upgrade

- Hardware: → all hardware production/testing finished
  Custom: Pulsar, mezzanine cards, AUX, LVDS splitter
  Commercial: fiber splitter, SLINK mezzanine, SLINK-PCI cards,
  Linux processors
- Firmware: → all firmware in place, fine tuning started
  Transmitters and receivers for all data paths
  SLINK merger and L2 to trigger supervisor interfaces
  → about 14 different types of Pulsar firmware
  Keys to success: uniformity modularity, CVS control, dedicated writers
- Software: → core software in place, fine tuning started
  board testing, VME DAQ readout, online/offline monitoring,
  infrastructure software for decision PC and L2 algorithm…
- Beam tests: → started June 2004
  beam tests → monitoring → firmware/software fine tuning

Run IIa Track Trigger System

- XFT works by finding line segments in the four axial superlayers
  - "finder" boards
- Tracks are found by linking the segments into tracks
  - "linker" boards

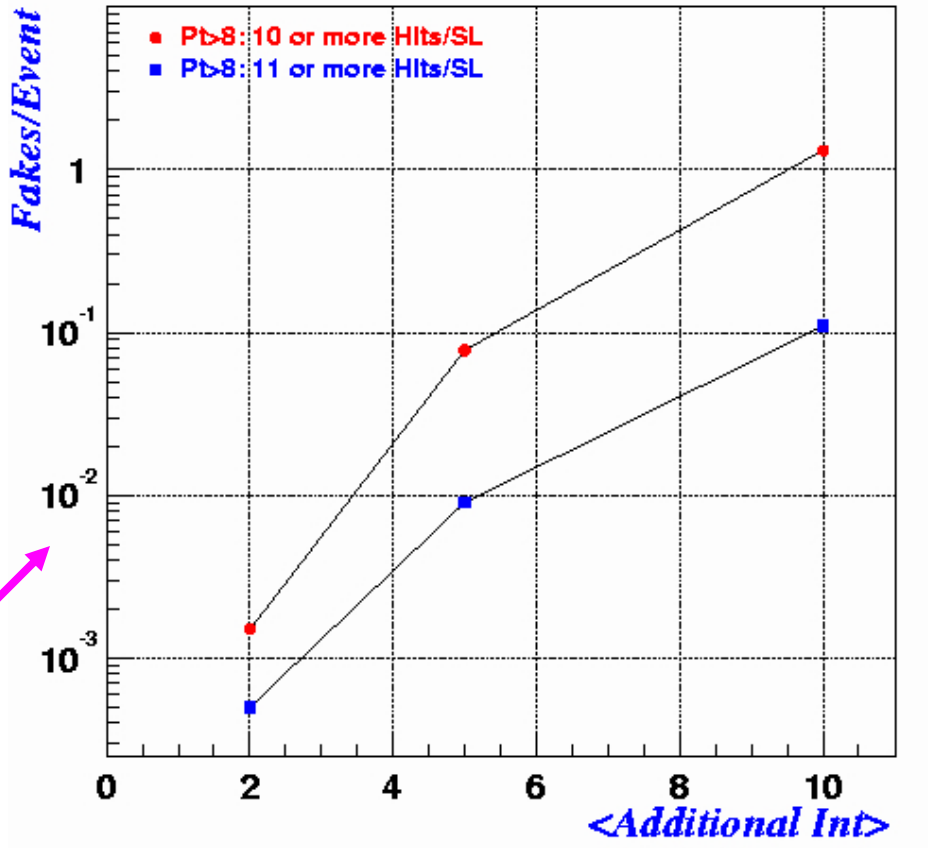


Interaction point

XFT Upgrade

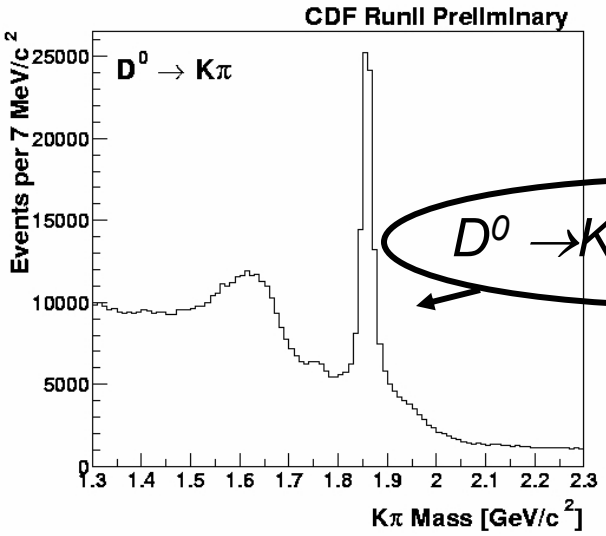
From Sep. 2002 DOE Review

- Track-based triggers are responsible for >50% of the Run IIb physics program
  - e, μ, τ, *b*-tags
- COT occupancy at high luminosity causes significant L1 track trigger (XFT) degradation
  - Significant growth in fake track rate (primarily at high p_T)
  - Significant degradation in p_T and ϕ_0 resolution



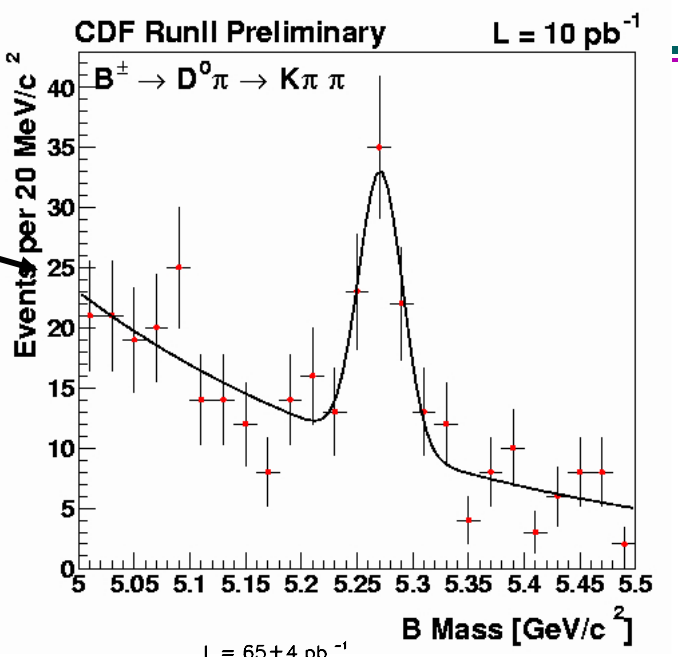
Minimum bias MC events

Run IIa SVT

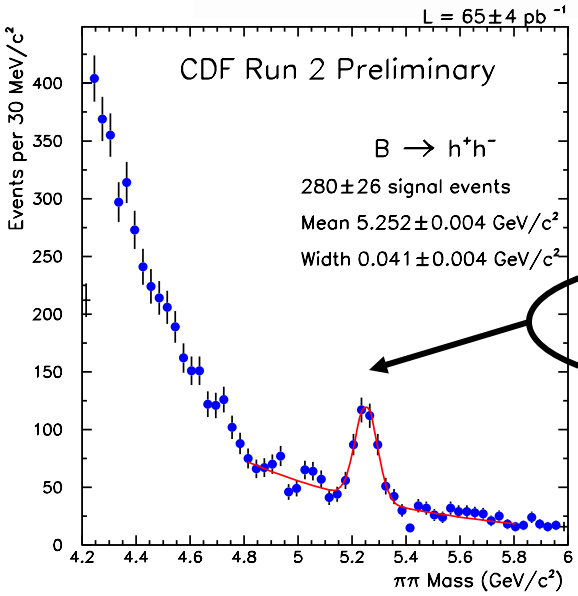


$B^+ \rightarrow D^0\pi^+$

$D^0 \rightarrow K^-\pi^+, K^-K^+, \pi^-\pi^+$



- Silicon tracking information in the trigger
  - find displaced tracks
  - Run IIb: important for Higgs, SUSY, $Z \rightarrow bb$
  - Also to continue – hadronic B_s decays



$B^0 \rightarrow h^+h^-$

Run 2A Readout/L3 Architecture